EE 330
Lecture 5

Statistics Review (continued)

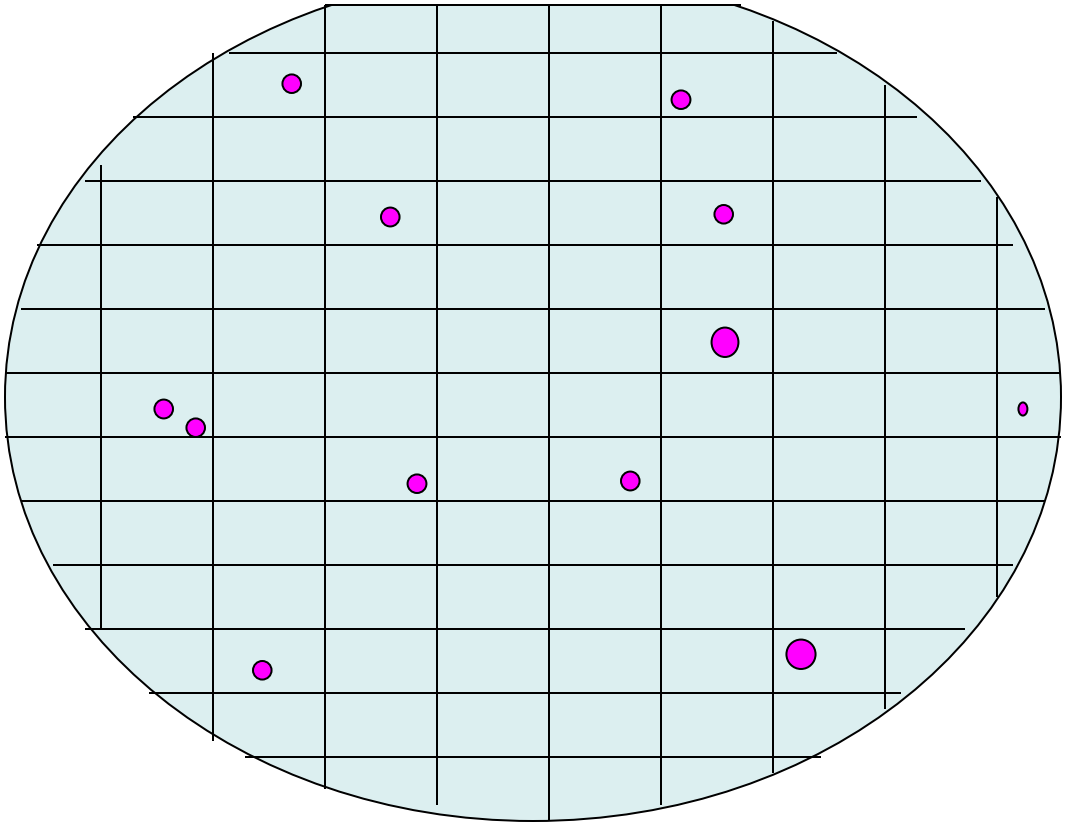
Key Historical Developments

As a courtesy to fellow classmates, TAs, and the instructor

Wearing of masks during lectures and in the laboratories for this course would be appreciated irrespective of vaccination status

Review from Last Lecture

Defects in a Wafer



- Dust particles and other undesirable processes cause defects
- Defects in manufacturing cause yield loss

Review from Last Lecture

Hard Fault Model

$$Y_H = e^{-Ad}$$

Y_H is the probability that the die does not have a hard fault
A is the die area
d is the defect density (typically $1cm^{-2} < d < 2cm^{-2}$)

Industry often closely guards the value of d for their process

Other models, which may be better, have the same general functional form

Overall Yield

If both hard and soft faults affect the yield of a circuit, the overall yield is given by the expression

$$Y = Y_H Y_S$$

Review from Last Lecture

Cost Per Good Die

The manufacturing costs per good die is given by

$$C_{Good} = \frac{C_{FabDie}}{Y}$$

where C_{FabDie} is the manufacturing costs of a fab die and Y is the yield

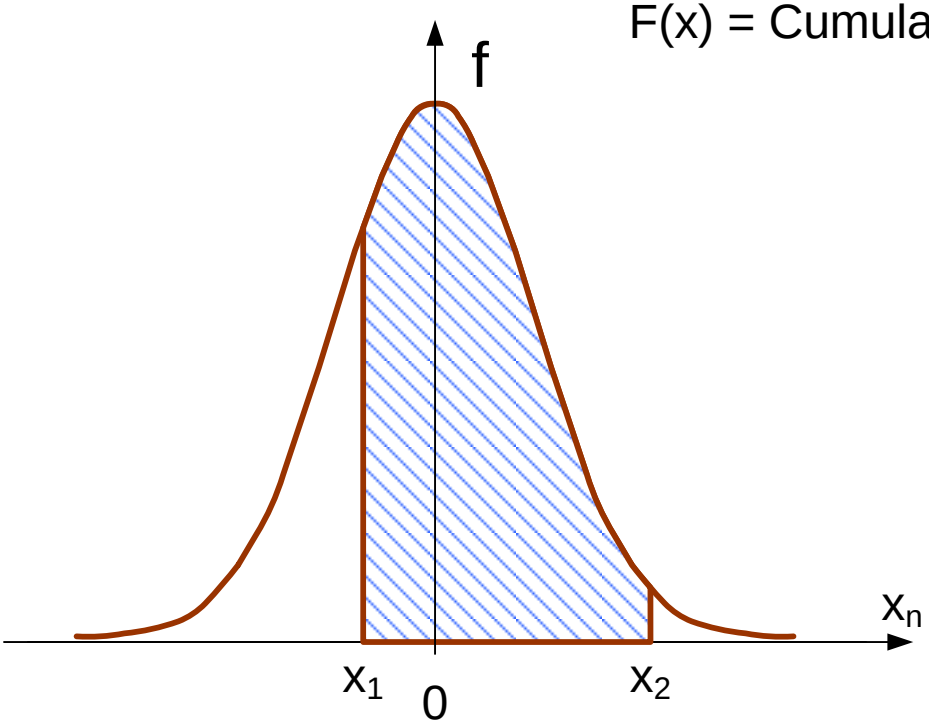
There are other costs that must ultimately be included such as testing costs, engineering costs, etc.

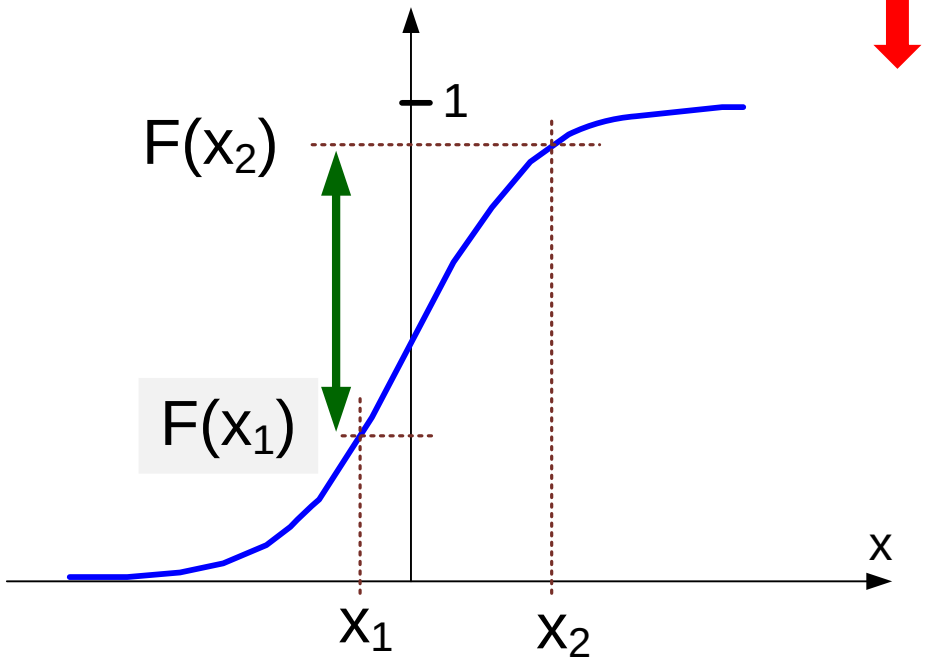
Review from Last Lecture

Statistics Review

f(x) = Probability Density Function for x

F(x) = Cumulative Density Function for x



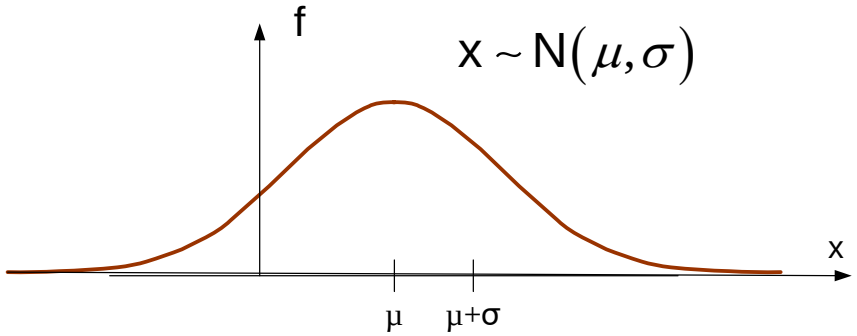


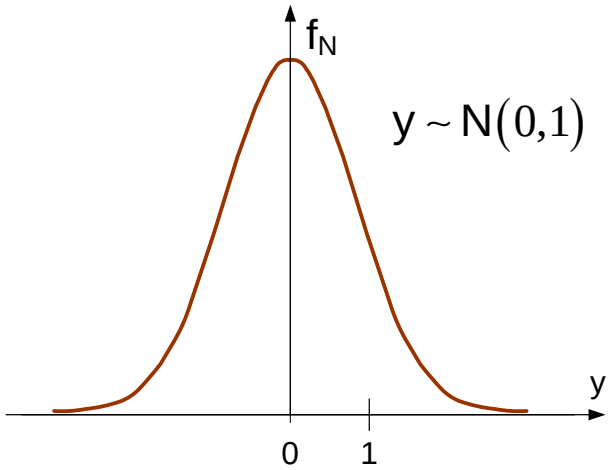
$$P\{X_1 \le x \le X_2\} = \int_{x_1}^{x_2} f(x)\,dx$$

$$P\{X_1 \le x \le X_2\} = F(X_2) - F(X_1)$$

Review from Last Lecture

Statistics Review





$$\int_{x=-\infty}^{\infty} f(x)\,dx = 1$$

$$y = \frac{x-\mu}{\sigma}$$

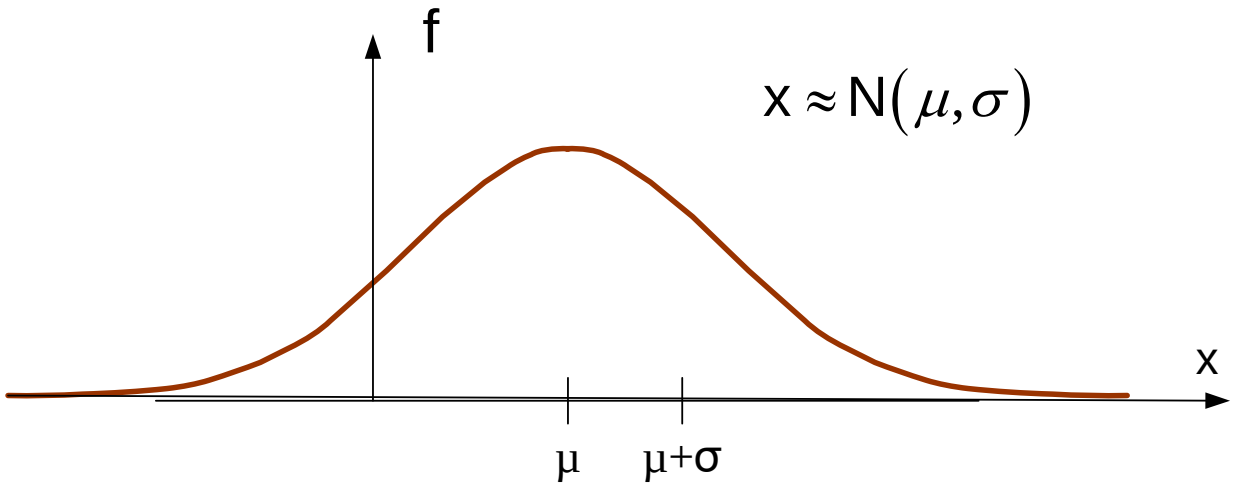
$$\int_{y=-\infty}^{\infty} f_N(y)\,dy = 1$$

Theorem 1: If the random variable x in normally distributed with mean μ and standard deviation σ, then $y = \frac{x-\mu}{\sigma}$ is also a random variable that is normally distributed with mean 0 and standard deviation of 1.

(Normal Distribution and Gaussian Distribution are the same)

Review from Last Lecture

Statistics Review

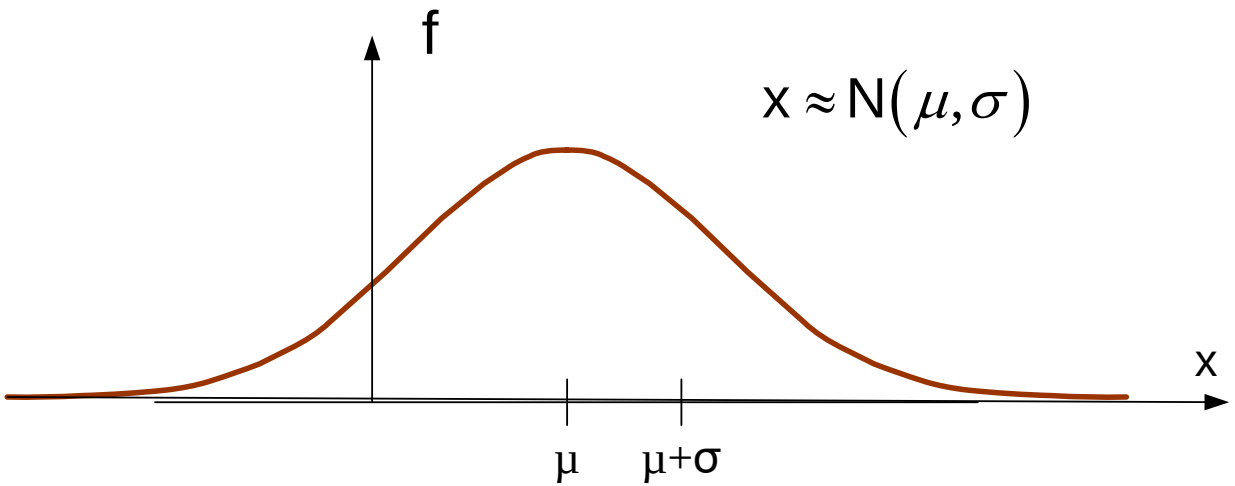


The random part of many parameters of microelectronic circuits is often assumed to be Normally distributed and experimental observations confirm that this assumption provides close agreement between theoretical and experimental results

The mapping $y = \frac{x - \mu}{\sigma}$ is often used to simplify the statistical characterization of the random parameters in microelectronic circuits

x generally is dimensioned, y is dimensionless

Statistics Review



Example:

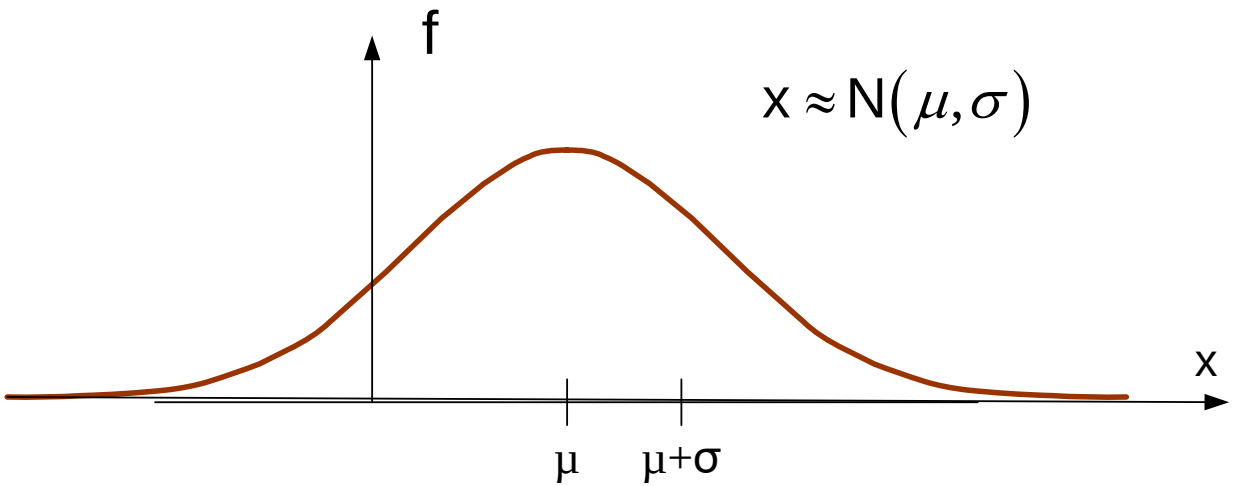
x might be the frequency of oscillation of a ring oscillator used for a clock in a crystal-less digital circuit, x Gaussian (Normal)

Dimensions of x : Hz
Maybe μ=550 MHz σ=50 MHz

$$y = \frac{x - \mu}{\sigma}$$ is dimensionless with $\mu_y=0$ $\sigma_y=1$

y: N(0,1)

Statistics Review



Example:

x might be the offset voltage of an op amp, x Gaussian (Normal)

Dimensions of x : Volts
Typically μ=0V σ=10 mV

$$y = \frac{x-\mu}{\sigma}$$ is dimensionless with $\mu_y=0$ $\sigma_y=1$

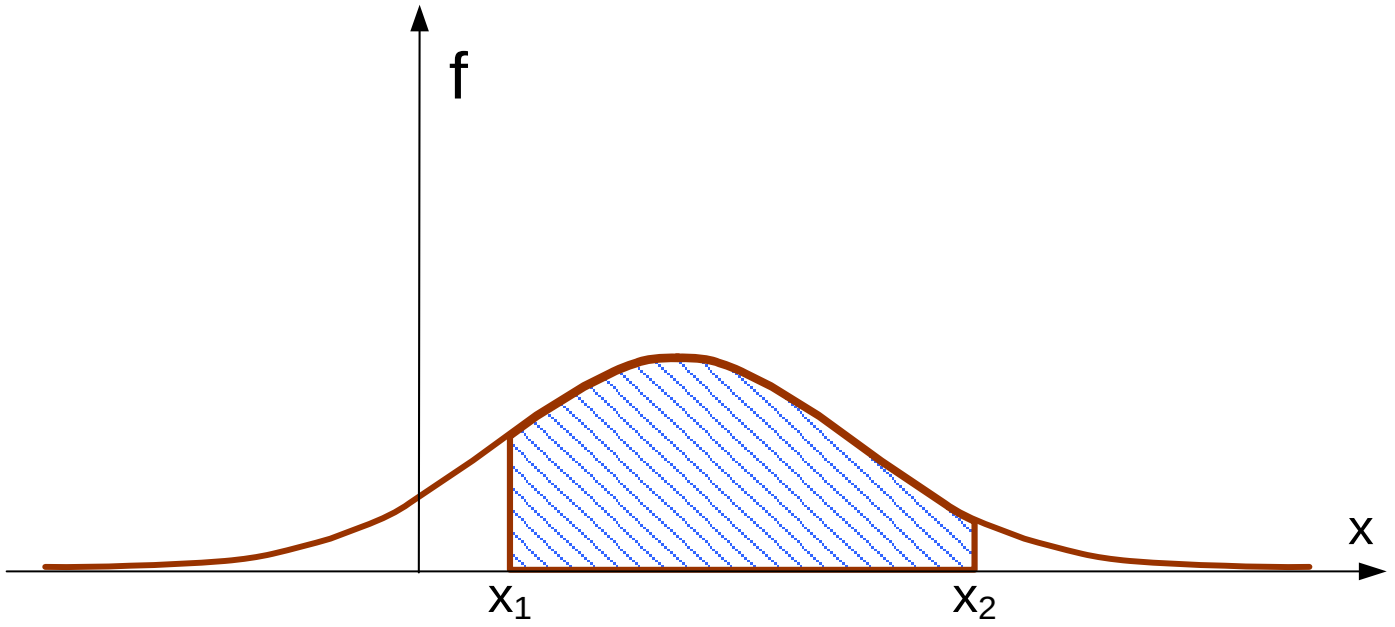
y: N(0,1)

Background Information

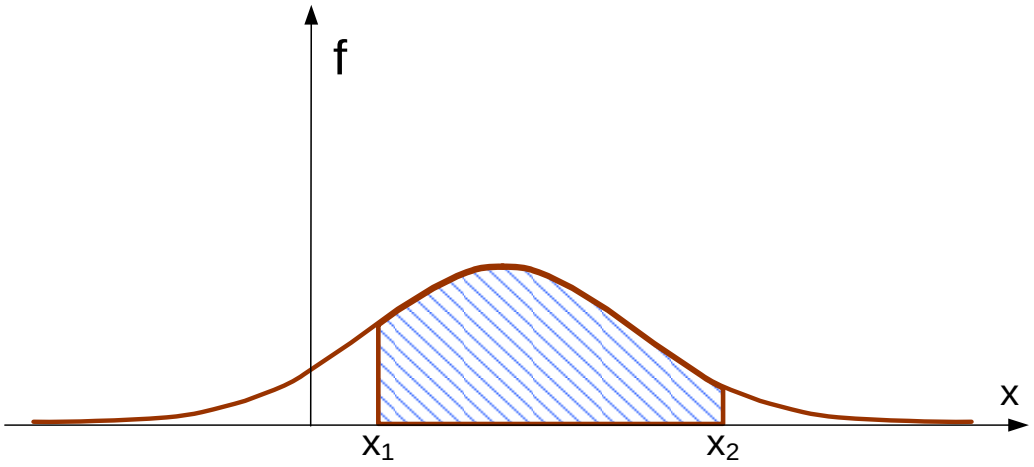
Theorem 2: If x is a Normal (Gaussian) random variable with mean μ and standard deviation σ, then the probability that x is between x_1 and x_2 is given by

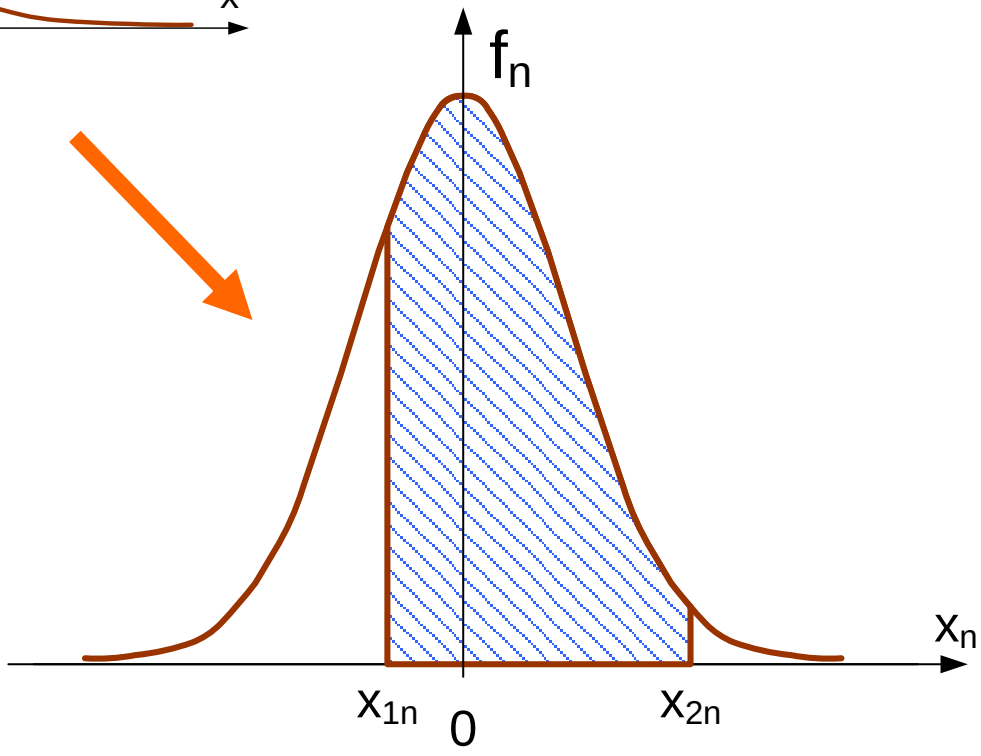
$$p = \int_{x_1}^{x_2} f(x)\,dx = \int_{x_{1n}}^{x_{2n}} f_n(x)\,dx \quad \text{where} \quad x_{1n} = \frac{x_1 - \mu}{\sigma} \quad \text{and} \quad x_{2n} = \frac{x_2 - \mu}{\sigma}$$

and where $f_n(x)$ is N(0,1)



Background Information



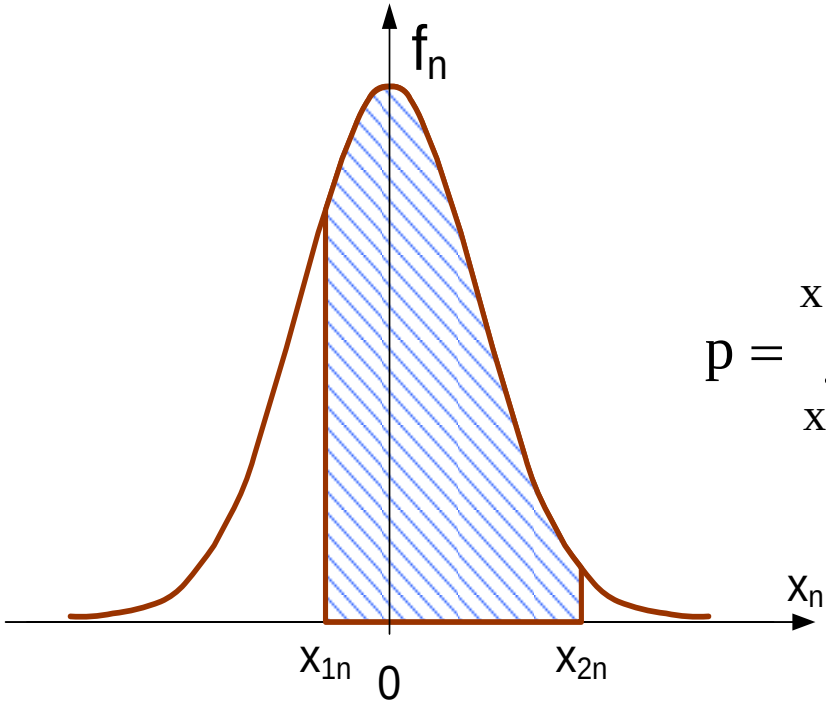


Background Information

Observation: The probability that the N(0,1) random variable x_n satisfies the relationship $x_{1n}<x_n<x_{2n}$ is also given by

$$p = F_n\left(x_{2n}\right) - F_n\left(x_{1n}\right)$$

where $F_n(x)$ is the CDF of x_n.



$$p = \int_{x_{1n}}^{x_{2n}} f_n\left(x\right) dx$$

Since the N(0,1) distribution is symmetric around 0, p can also be expressed as

$$p = F_n\left(x_{2n}\right) - \left(1 - F_n\left(-x_{1n}\right)\right)$$

Background Information

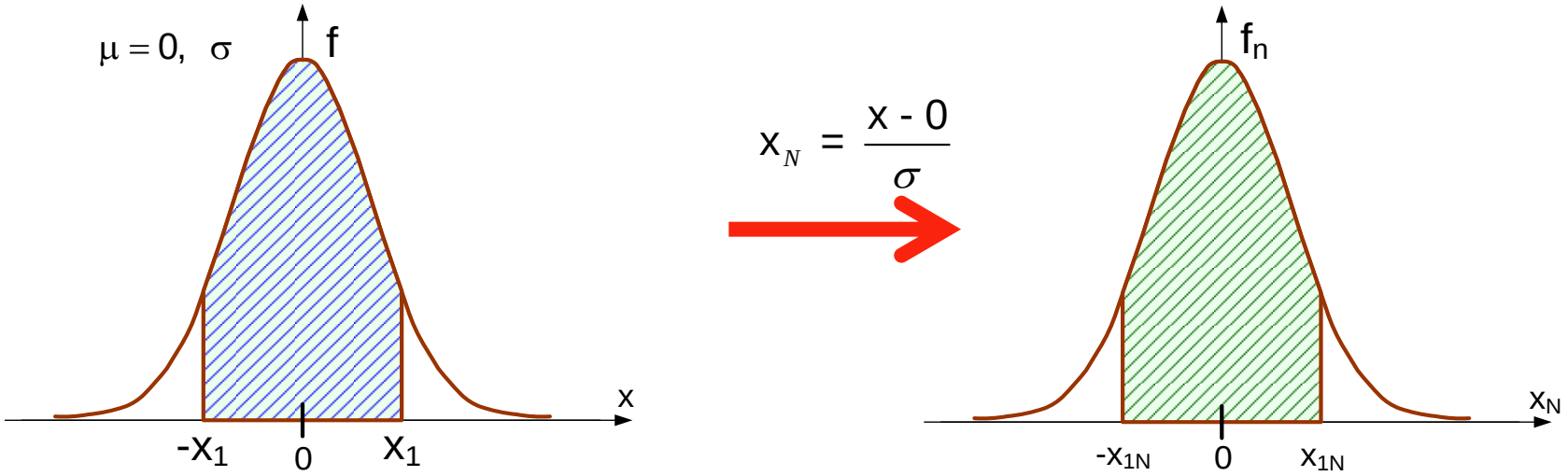
Observation: In many electronic circuits, a random variable of interest, x, is 0 mean Gaussian and the probabilities of interest are characterized by a region defined by the <u>magnitude</u> of the random variable (i.e. $-x_1 < x < x_1$).

In these cases, if we define $x_N = \frac{x - 0}{\sigma}$ then x_N is N(0,1) and

$$p(-x_1 < x < x_1) = \int_{-x_1}^{x_1} f(x)\,dx = \int_{-x_{1n}}^{x_{1n}} f_n(x)\,dx = F_n(x_{1n}) - F_n(-x_{1n})$$

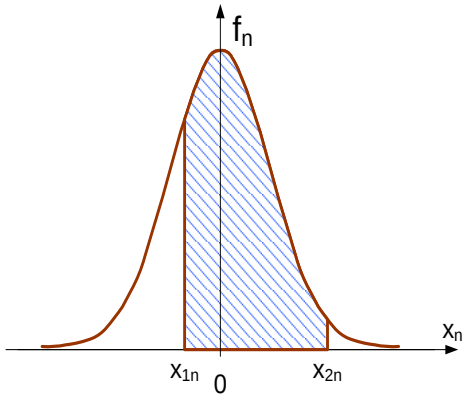
But for the N(0,1) distribution $F_n(-x_{1n}) = 1 - F_n(x_{1n})$

therefore: $p = 2F_n(x_{1n}) - 1$

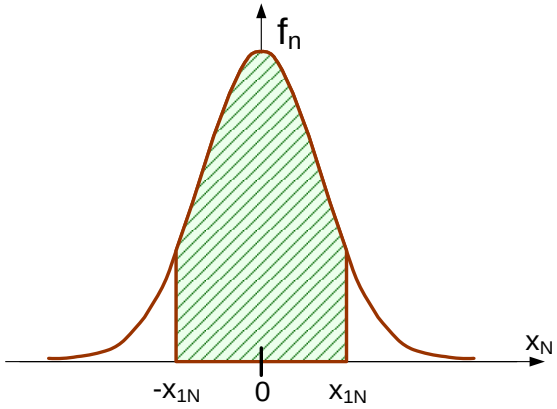


Background Information

$$p = F_n\left(x_{2n}\right) - F_n\left(x_{1n}\right)$$



$$p = 2F_n\left(x_{1n}\right) - 1$$



Regardless of whether Gaussian performance requirements are asymmetric or symmetric, the CDF of the N(0,1) distribution (i.e. $F_n(x_n)$) is used to characterize yield

Background Information

Tables of the CDF of the N(0,1) random variable are readily available. It is also available in Matlab, Excel, and a host of other sources.

Probability Content from -oo to Z

Z	0.00	0.01	0.02	0.03	0.04	0.05	0.06	0.07	0.08	0.09
0.0	0.5000	0.5040	0.5080	0.5120	0.5160	0.5199	0.5239	0.5279	0.5319	0.5359
0.1	0.5398	0.5438	0.5478	0.5517	0.5557	0.5596	0.5636	0.5675	0.5714	0.5753
0.2	0.5793	0.5832	0.5871	0.5910	0.5948	0.5987	0.6026	0.6064	0.6103	0.6141
0.3	0.6179	0.6217	0.6255	0.6293	0.6331	0.6368	0.6406	0.6443	0.6480	0.6517
0.4	0.6554	0.6591	0.6628	0.6664	0.6700	0.6736	0.6772	0.6808	0.6844	0.6879
0.5	0.6915	0.6950	0.6985	0.7019	0.7054	0.7088	0.7123	0.7157	0.7190	0.7224
0.6	0.7257	0.7291	0.7324	0.7357	0.7389	0.7422	0.7454	0.7486	0.7517	0.7549
0.7	0.7580	0.7611	0.7642	0.7673	0.7704	0.7734	0.7764	0.7794	0.7823	0.7852
0.8	0.7881	0.7910	0.7939	0.7967	0.7995	0.8023	0.8051	0.8078	0.8106	0.8133
0.9	0.8159	0.8186	0.8212	0.8238	0.8264	0.8289	0.8315	0.8340	0.8365	0.8389
1.0	0.8413	0.8438	0.8461	0.8485	0.8508	0.8531	0.8554	0.8577	0.8599	0.8621
1.1	0.8643	0.8665	0.8686	0.8708	0.8729	0.8749	0.8770	0.8790	0.8810	0.8830
1.2	0.8849	0.8869	0.8888	0.8907	0.8925	0.8944	0.8962	0.8980	0.8997	0.9015
1.3	0.9032	0.9049	0.9066	0.9082	0.9099	0.9115	0.9131	0.9147	0.9162	0.9177
1.4	0.9192	0.9207	0.9222	0.9236	0.9251	0.9265	0.9279	0.9292	0.9306	0.9319
1.5	0.9332	0.9345	0.9357	0.9370	0.9382	0.9394	0.9406	0.9418	0.9429	0.9441
1.6	0.9452	0.9463	0.9474	0.9484	0.9495	0.9505	0.9515	0.9525	0.9535	0.9545
1.7	0.9554	0.9564	0.9573	0.9582	0.9591	0.9599	0.9608	0.9616	0.9625	0.9633
1.8	0.9641	0.9649	0.9656	0.9664	0.9671	0.9678	0.9686	0.9693	0.9699	0.9706
1.9	0.9713	0.9719	0.9726	0.9732	0.9738	0.9744	0.9750	0.9756	0.9761	0.9767
2.0	0.9772	0.9778	0.9783	0.9788	0.9793	0.9798	0.9803	0.9808	0.9812	0.9817
2.1	0.9821	0.9826	0.9830	0.9834	0.9838	0.9842	0.9846	0.9850	0.9854	0.9857
2.2	0.9861	0.9864	0.9868	0.9871	0.9875	0.9878	0.9881	0.9884	0.9887	0.9890
2.3	0.9893	0.9896	0.9898	0.9901	0.9904	0.9906	0.9909	0.9911	0.9913	0.9916
2.4	0.9918	0.9920	0.9922	0.9925	0.9927	0.9929	0.9931	0.9932	0.9934	0.9936
2.5	0.9938	0.9940	0.9941	0.9943	0.9945	0.9946	0.9948	0.9949	0.9951	0.9952
2.6	0.9953	0.9955	0.9956	0.9957	0.9959	0.9960	0.9961	0.9962	0.9963	0.9964
2.7	0.9965	0.9966	0.9967	0.9968	0.9969	0.9970	0.9971	0.9972	0.9973	0.9974
2.8	0.9974	0.9975	0.9976	0.9977	0.9977	0.9978	0.9979	0.9979	0.9980	0.9981
2.9	0.9981	0.9982	0.9982	0.9983	0.9984	0.9984	0.9985	0.9985	0.9986	0.9986
3.0	0.9987	0.9987	0.9987	0.9988	0.9988	0.9989	0.9989	0.9989	0.9990	0.9990

http://www.math.unb.ca/~knight/utility/NormTble.htm

Background Information

Tables of the CDF of the N(0,1) random variable are readily available. It is also available in Matlab, Excel, and a host of other sources.

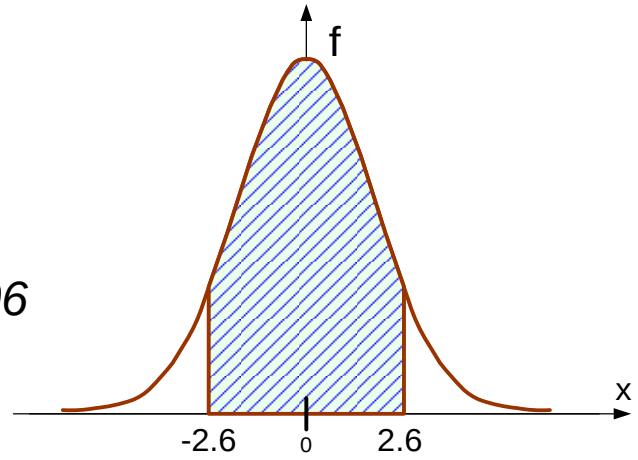
Far Right Tail Probabilities

Z	P{Z to oo}	Z	P{Z to oo}	Z	P{Z to oo}	Z	P{Z to oo}
2.0	0.02275	3.0	0.001350	4.0	0.00003167	5.0	2.867 E-7
2.1	0.01786	3.1	0.0009676	4.1	0.00002066	5.5	1.899 E-8
2.2	0.01390	3.2	0.0006871	4.2	0.00001335	6.0	9.866 E-10
2.3	0.01072	3.3	0.0004834	4.3	0.00000854	6.5	4.016 E-11
2.4	0.00820	3.4	0.0003369	4.4	0.000005413	7.0	1.280 E-12
2.5	0.00621	3.5	0.0002326	4.5	0.000003398	7.5	3.191 E-14
2.6	0.004661	3.6	0.0001591	4.6	0.000002112	8.0	6.221 E-16
2.7	0.003467	3.7	0.0001078	4.7	0.000001300	8.5	9.480 E-18
2.8	0.002555	3.8	0.00007235	4.8	7.933 E-7	9.0	1.129 E-19
2.9	0.001866	3.9	0.00004810	4.9	4.792 E-7	9.5	1.049 E-21

Background Information

Example: Determine the probability that the N(0,1) random variable has magnitude less than 2.6

$$p = 2F_n(2.6) - 1$$



From the table of the CDF, $F_n(2.6) = 0.9953$ so $p=.9906$

Probability Content from -oo to Z

Z	0.00	0.01	0.02	0.03	0.04	0.05	0.06	0.07	0.08	0.09
0.0	0.5000	0.5040	0.5080	0.5120	0.5160	0.5199	0.5239	0.5279	0.5319	0.5359
0.1	0.5398	0.5438	0.5478	0.5517	0.5557	0.5596	0.5636	0.5675	0.5714	0.5753
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0.3	0.6179	0.6217	0.6255	0.6293	0.6331	0.6368	0.6406	0.6443	0.6480	0.6517
0.4	0.6554	0.6591	0.6628	0.6664	0.6700	0.6736	0.6772	0.6808	0.6844	0.6879
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0.7	0.7580	0.7611	0.7642	0.7673	0.7704	0.7734	0.7764	0.7794	0.7823	0.7852
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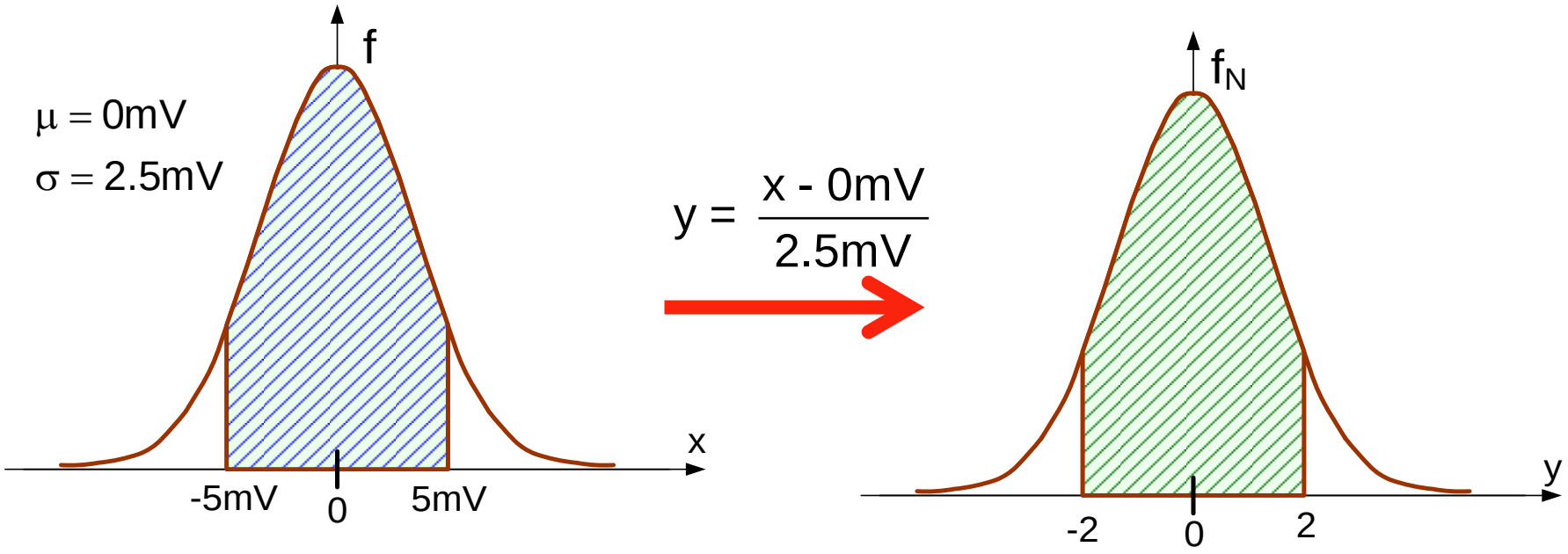
0.9	0.8159	0.8186	0.8212	0.8238	0.8264	0.8289	0.8315	0.8340	0.8365	0.8389
1.0	0.8413	0.8438	0.8461	0.8485	0.8508	0.8531	0.8554	0.8577	0.8599	0.8621
1.1	0.8643	0.8665	0.8686	0.8708	0.8729	0.8749	0.8770	0.8790	0.8810	0.8830
1.2	0.8849	0.8869	0.8888	0.8907	0.8925	0.8944	0.8962	0.8980	0.8997	0.9015
1.3	0.9032	0.9049	0.9066	0.9082	0.9099	0.9115	0.9131	0.9147	0.9162	0.9177
1.4	0.9192	0.9207	0.9222	0.9236	0.9251	0.9265	0.9279	0.9292	0.9306	0.9319
1.5	0.9332	0.9345	0.9357	0.9370	0.9382	0.9394	0.9406	0.9418	0.9429	0.9441
1.6	0.9452	0.9463	0.9474	0.9484	0.9495	0.9505	0.9515	0.9525	0.9535	0.9545
1.7	0.9554	0.9564	0.9573	0.9582	0.9591	0.9599	0.9608	0.9616	0.9625	0.9633
1.8	0.9641	0.9649	0.9656	0.9664	0.9671	0.9678	0.9686	0.9693	0.9699	0.9706
1.9	0.9713	0.9719	0.9726	0.9732	0.9738	0.9744	0.9750	0.9756	0.9761	0.9767
2.0	0.9772	0.9778	0.9783	0.9788	0.9793	0.9798	0.9803	0.9808	0.9812	0.9817
2.1	0.9821	0.9826	0.9830	0.9834	0.9838	0.9842	0.9846	0.9850	0.9854	0.9857
2.2	0.9861	0.9864	0.9868	0.9871	0.9875	0.9878	0.9881	0.9884	0.9887	0.9890
2.3	0.9893	0.9896	0.9898	0.9901	0.9904	0.9906	0.9909	0.9911	0.9913	0.9916
2.4	0.9918	0.9920	0.9922	0.9925	0.9927	0.9929	0.9931	0.9932	0.9934	0.9936
2.5	[illegible]	0.9940	0.9941	0.9943	0.9945	0.9946	0.9948	0.9949	0.9951	0.9952
2.6	0.9953	0.9955	0.9956	0.9957	0.9959	0.9960	0.9961	0.9962	0.9963	0.9964
2.7	[illegible]	0.9966	0.9967	0.9968	0.9969	0.9970	0.9971	0.9972	0.9973	0.9974
2.8	0.9974	0.9975	0.9976	0.9977	0.9977	0.9978	0.9979	0.9979	0.9980	0.9981
2.9	0.9981	0.9982	0.9982	0.9983	0.9984	0.9984	0.9985	0.9985	0.9986	0.9986
3.0	0.9987	0.9987	0.9987	0.9988	0.9988	0.9989	0.9989	0.9989	0.9990	0.9990

Background Information

It can be shown that the circuit designer has control of the offset voltage of an op amp and through architecture and sizing of devices can set the standard deviation of the offset voltage at almost any level. Invariably low offset voltages require larger area.

Example: Determine the soft yield of an operational amplifier that has an offset voltage requirement of 5mV if the offset voltage has a Gaussian distribution with a standard deviation of 2.5mV and a mean of 0V.



$$p = \int_{-2}^{2} f_N(x)\,dx = F_N(2) - F_N(-2) = 2 * F_N(2) - 1$$

$$p = 2 * F_N(2) - 1$$

Example (continued)

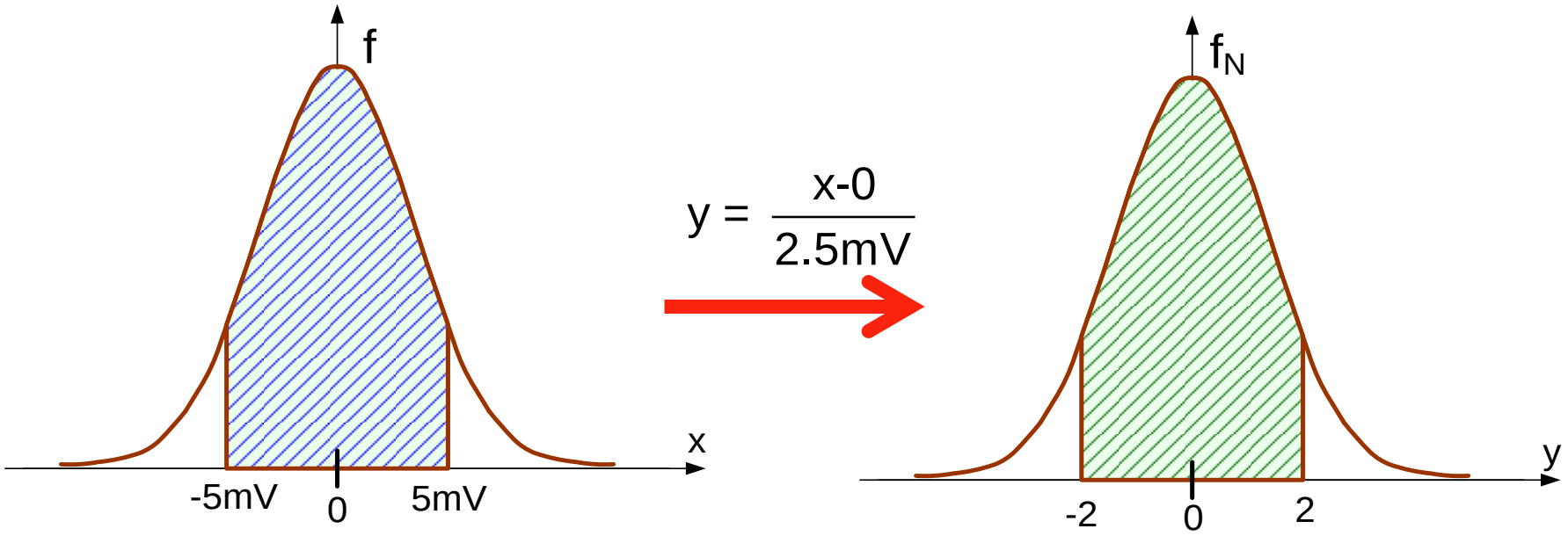
Probability Content from -oo to Z

Z	0.00	0.01	0.02	0.03	0.04	0.05	0.06	0.07	0.08	0.09
0.0	0.5000	0.5040	0.5080	0.5120	0.5160	0.5199	0.5239	0.5279	0.5319	0.5359
0.1	0.5398	0.5438	0.5478	0.5517	0.5557	0.5596	0.5636	0.5675	0.5714	0.5753
0.2	0.5793	0.5832	0.5871	0.5910	0.5948	0.5987	0.6026	0.6064	0.6103	0.6141
0.3	0.6179	0.6217	0.6255	0.6293	0.6331	0.6368	0.6406	0.6443	0.6480	0.6517
0.4	0.6554	0.6591	0.6628	0.6664	0.6700	0.6736	0.6772	0.6808	0.6844	0.6879
0.5	0.6915	0.6950	0.6985	0.7019	0.7054	0.7088	0.7123	0.7157	0.7190	0.7224
0.6	0.7257	0.7291	0.7324	0.7357	0.7389	0.7422	0.7454	0.7486	0.7517	0.7549
0.7	0.7580	0.7611	0.7642	0.7673	0.7704	0.7734	0.7764	0.7794	0.7823	0.7852
0.8	0.7881	0.7910	0.7939	0.7967	0.7995	0.8023	0.8051	0.8078	0.8106	0.8133
0.9	0.8159	0.8186	0.8212	0.8238	0.8264	0.8289	0.8315	0.8340	0.8365	0.8389
1.0	0.8413	0.8438	0.8461	0.8485	0.8508	0.8531	0.8554	0.8577	0.8599	0.8621
1.1	0.8643	0.8665	0.8686	0.8708	0.8729	0.8749	0.8770	0.8790	0.8810	0.8830
1.2	0.8849	0.8869	0.8888	0.8907	0.8925	0.8944	0.8962	0.8980	0.8997	0.9015
1.3	0.9032	0.9049	0.9066	0.9082	0.9099	0.9115	0.9131	0.9147	0.9162	0.9177
1.4	0.9192	0.9207	0.9222	0.9236	0.9251	0.9265	0.9279	0.9292	0.9306	0.9319
1.5	0.9332	0.9345	0.9357	0.9370	0.9382	0.9394	0.9406	0.9418	0.9429	0.9441
1.6	0.9452	0.9463	0.9474	0.9484	0.9495	0.9505	0.9515	0.9525	0.9535	0.9545
1.7	0.9554	0.9564	0.9573	0.9582	0.9591	0.9599	0.9608	0.9616	0.9625	0.9633
1.8	0.9641	0.9649	0.9656	0.9664	0.9671	0.9678	0.9686	0.9693	0.9699	0.9706
1.9	0.9713	0.9719	0.9726	0.9732	0.9738	0.9744	0.9750	0.9756	0.9761	0.9767
2.0	0.9772	0.9778	0.9783	0.9788	0.9793	0.9798	0.9803	0.9808	0.9812	0.9817
2.1	0.9821	0.9826	0.9830	0.9834	0.9838	0.9842	0.9846	0.9850	0.9854	0.9857
2.2	0.9861	0.9864	0.9868	0.9871	0.9875	0.9878	0.9881	0.9884	0.9887	0.9890
2.3	0.9893	0.9896	0.9898	0.9901	0.9904	0.9906	0.9909	0.9911	0.9913	0.9916
2.4	0.9918	0.9920	0.9922	0.9925	0.9927	0.9929	0.9931	0.9932	0.9934	0.9936
2.5	0.9938	0.9940	0.9941	0.9943	0.9945	0.9946	0.9948	0.9949	0.9951	0.9952
2.6	0.9953	0.9955	0.9956	0.9957	0.9959	0.9960	0.9961	0.9962	0.9963	0.9964
2.7	0.9965	0.9966	0.9967	0.9968	0.9969	0.9970	0.9971	0.9972	0.9973	0.9974
2.8	0.9974	0.9975	0.9976	0.9977	0.9977	0.9978	0.9979	0.9979	0.9980	0.9981
2.9	0.9981	0.9982	0.9982	0.9983	0.9984	0.9984	0.9985	0.9985	0.9986	0.9986
3.0	0.9987	0.9987	0.9987	0.9988	0.9988	0.9989	0.9989	0.9989	0.9990	0.9990

http://www.math.unb.ca/~knight/utility/NormTble.htm

Example (continued)

Determine the soft yield of an operational amplifier that has an offset voltage requirement of 5mV if the offset voltage has a Gaussian distribution with a standard deviation of 2.5mV and a mean of 0V.



$$p = 2 * F_N(2) - 1$$

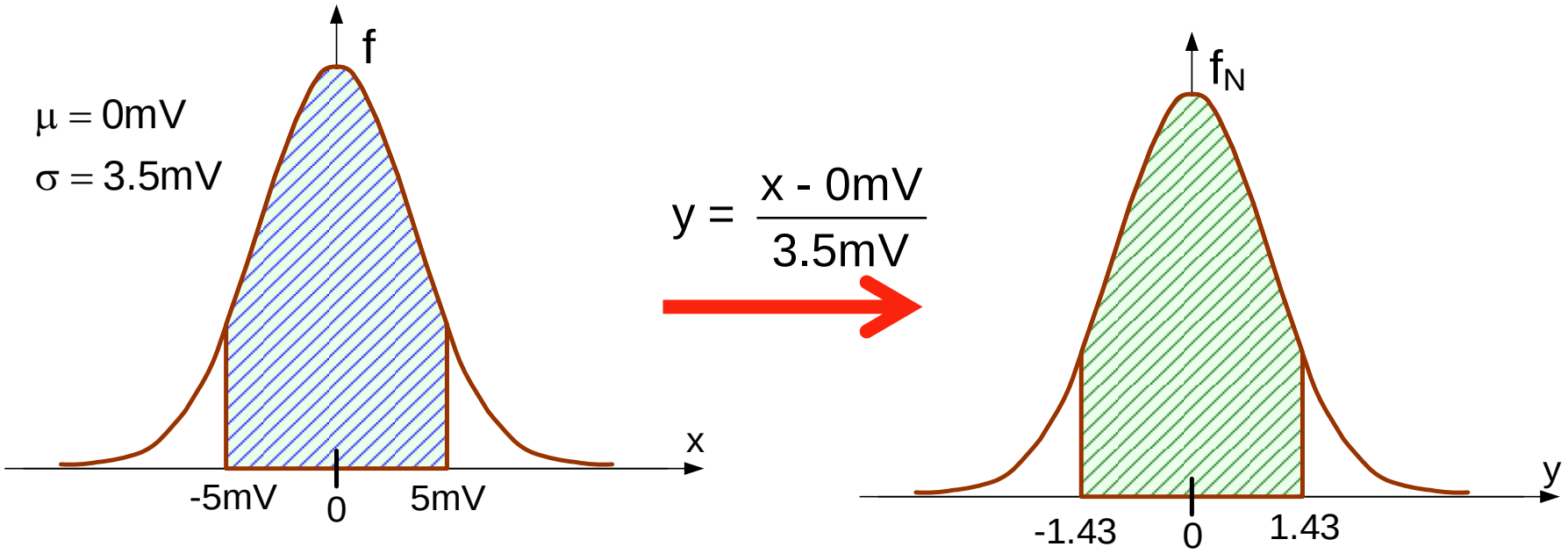
$$F_N(2) = 0.9772$$

$$p = 2 * .9772 - 1 = .9544$$

Background Information

Repeat the previous example if the designer decided to reduce the area so that the standard deviation increased to 3.5 mV

Example: Determine the soft yield of an operational amplifier that has an offset voltage requirement of 5mV if the offset voltage has a Gaussian distribution with a standard deviation of 3.5mV and a mean of 0V.



$$p = \int_{-1.43}^{1.43} f_N(x)\,dx = F_N(1.43) - F_N(-1.43) = 2 * F_N(1.43) - 1$$

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Background Information

Example (continued)

Probability Content from -oo to Z

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2.8	0.9974	0.9975	0.9976	0.9977	0.9977	0.9978	0.9979	0.9979	0.9980	0.9981
2.9	0.9981	0.9982	0.9982	0.9983	0.9984	0.9984	0.9985	0.9985	0.9986	0.9986
3.0	0.9987	0.9987	0.9987	0.9988	0.9988	0.9989	0.9989	0.9989	0.9990	0.9990

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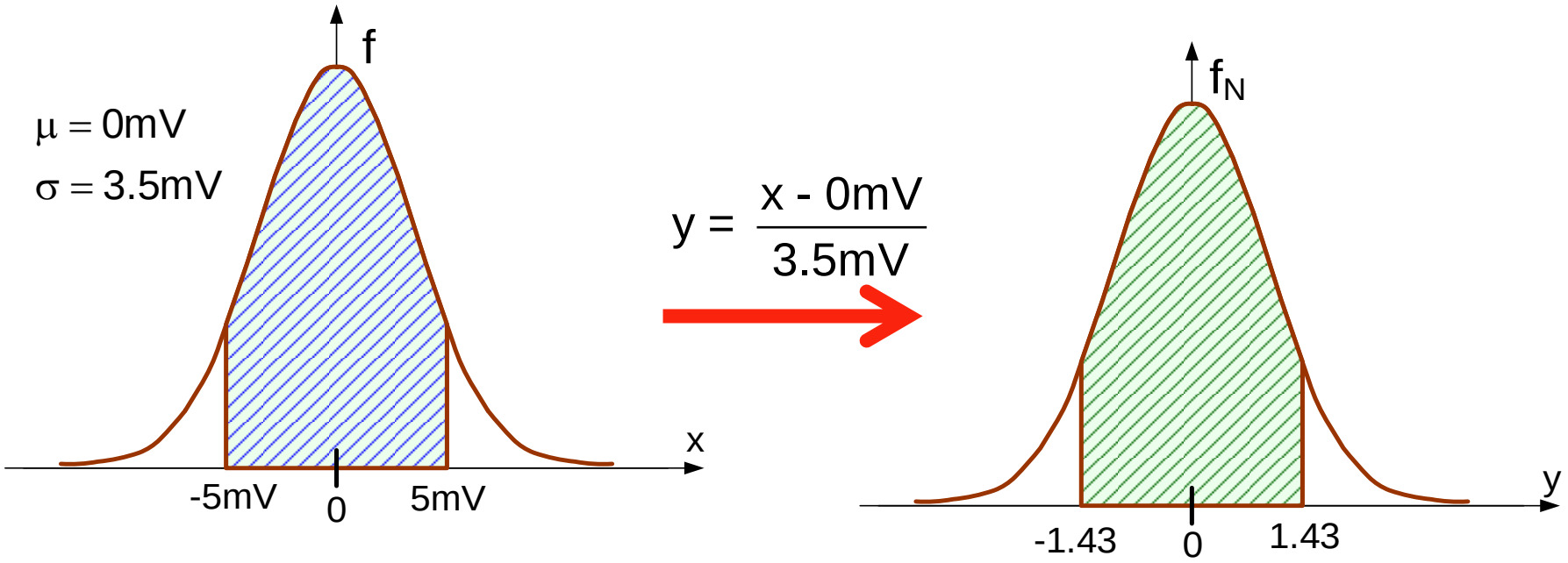
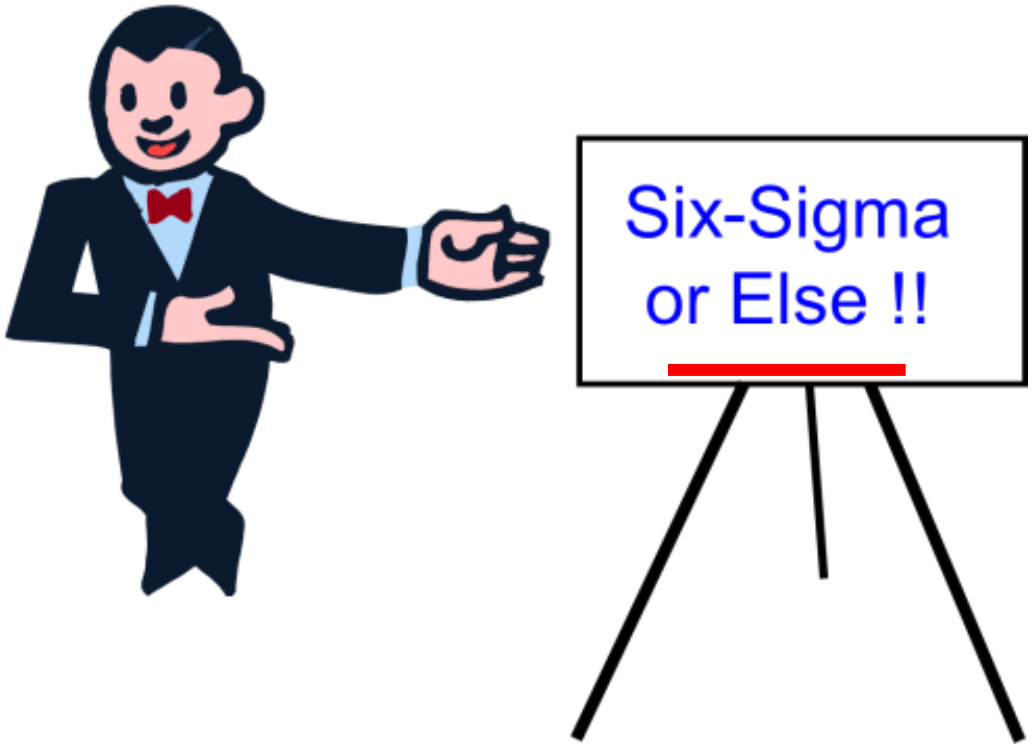


$$p = 2 * F_N(1.43) - 1 = 2 * 0.9236 - 1 = 0.847$$

This small change in the design dropped the yield from just over 95% to just under 85%

Statistical analysis is critical for predicting performance capabilities of many ICs !

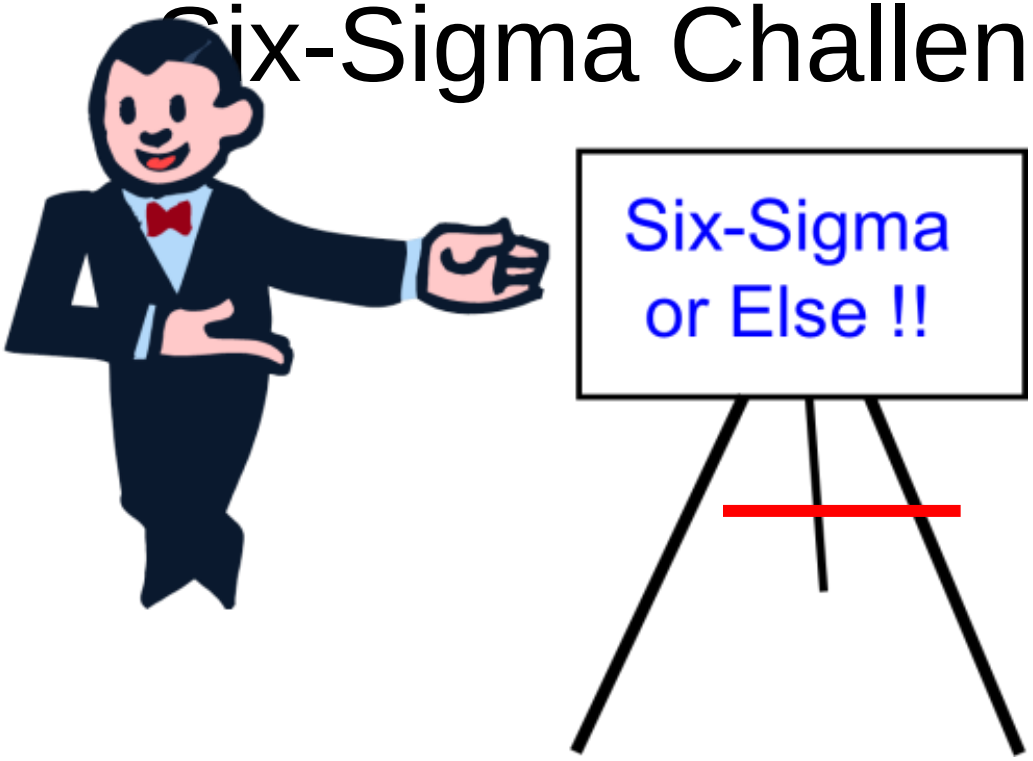
Many Companies Promote the Real Six-Sigma Challenge



From Wikipedia Sept 1 2021

Six Sigma (**6σ**) is a set of techniques and tools for process improvement. It was introduced by American engineer Bill Smith while working at Motorola in 1986.[1][2] A six sigma process is one in which 99.99966% of all opportunities to produce some feature of a part are statistically expected to be free of defects.

Many Companies Promote the Real Six-Sigma Challenge



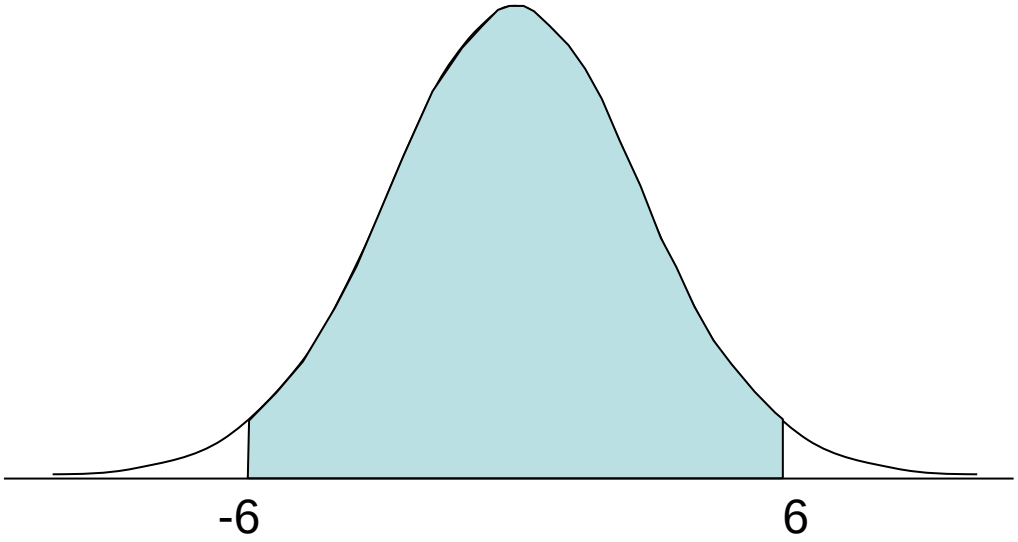
From Wikipedia Sept 1 2021

In 2005 Motorola attributed over $17 billion in savings to Six Sigma.[3]

By the late 1990s, about two-thirds of the Fortune 500 organizations had begun Six Sigma initiatives with the aim of reducing costs and improving quality.[6]

Yield at the Six-Sigma level

(Assume a Gaussian distribution)

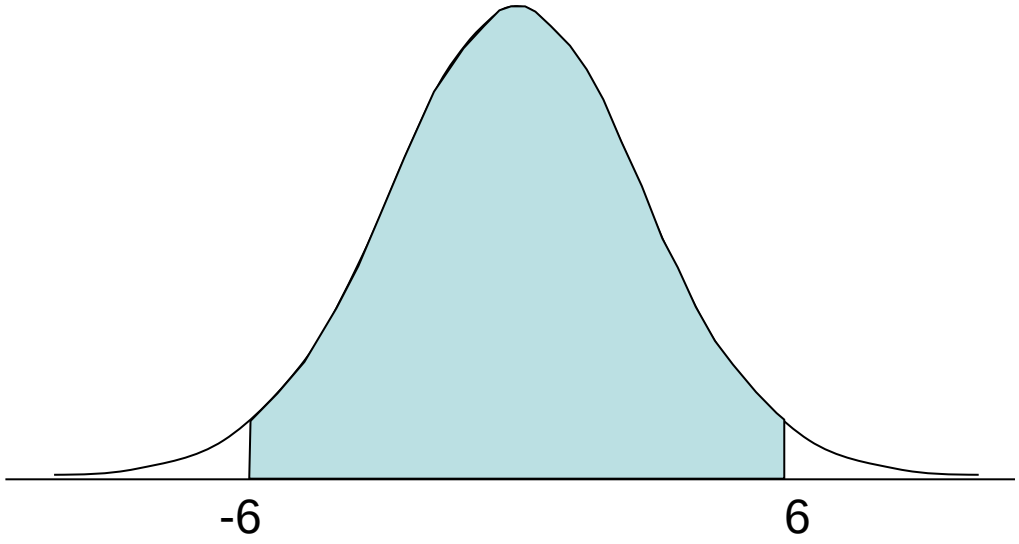


$$Y_{6sigma} = 2F_N(6) - 1$$

$$Y_{6sigma} = 0.9999999980$$

This is approximately 2 defects out of 1 billion parts

Yield at the Six-Sigma level



This is approximately 2 defects out of 1 billion parts

Would producing ICs with a yield at the six-sigma level be a good goal?

How about smart phones with defects at this level? (approx. 1.4B sold in 2020)

How about automobiles? (approx. 78 million produced in 2020)

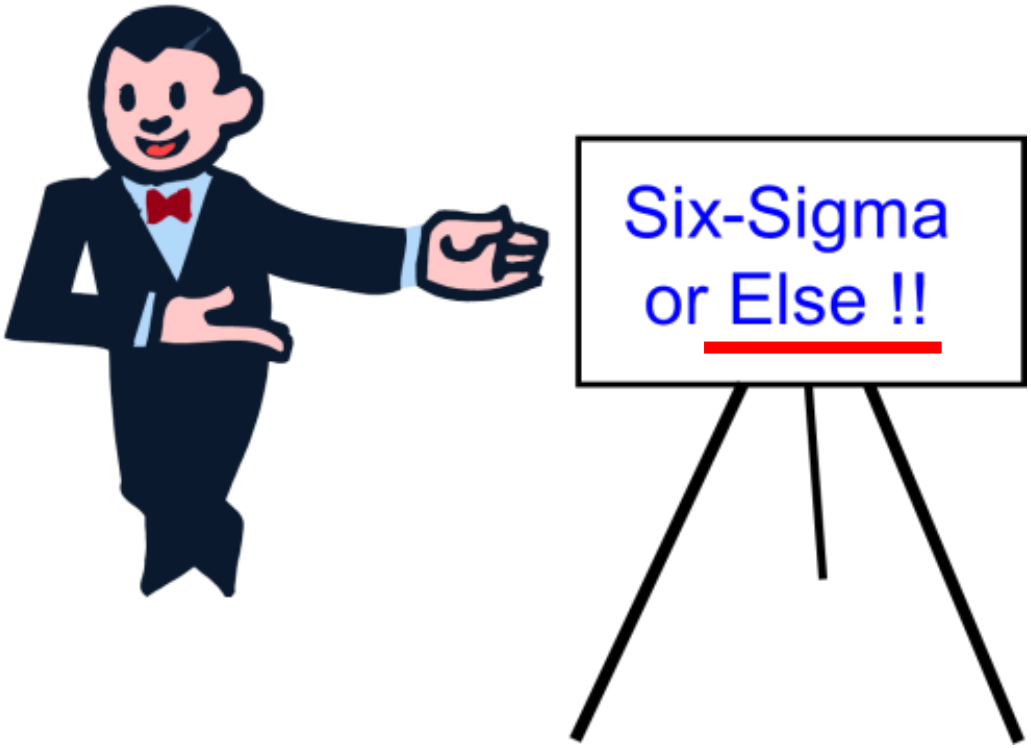
Six-Sigma or Else !!

How serious is the “or Else” in the six-sigma programs?

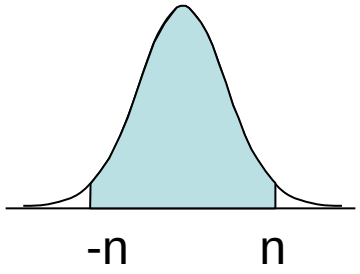
Genre	Reality game show
Created by	Mark Burnett
Composer(s)	David Vanacore (Vanacore Music), Jeff Lippencott and Mark T. Williams, Ah2 Music
Country of origin	United States
Production	
Executive producer(s)	Mark Burnett, Donald J. Trump, Jay Bienstock
Release	
Original network	NBC
Original release	January 8, 2004 – present

This is not a political advertisement !!

Meeting the Real Six-Sigma Challenge

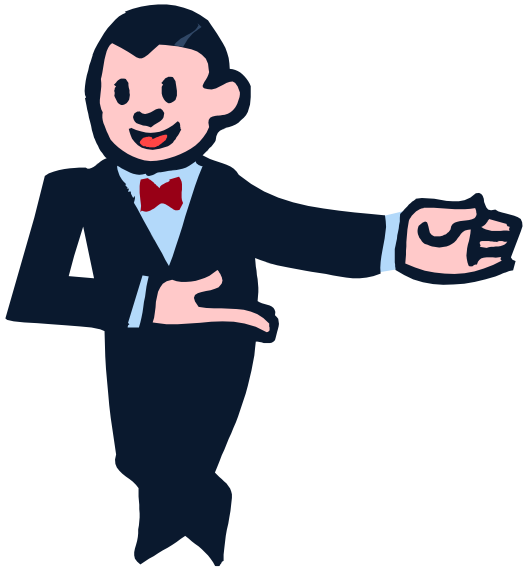


Yield at Various Sigma Levels



No Sigma	Yield	Defect Rate
1	0.682689492	0.317311
2	0.954499736	0.0455
3	0.997300204	0.0027
4	0.999936658	6.33E-05
5	0.999999427	5.73E-07
6	0.9999999980	1.97E-09
7	0.999999999974	2.56E-12

Six-sigma performance is approximately 2 defects in a billion !



Six-Sigma or Else !!

It is assumed that the performance or yield will drop, for some reason, by 1.5 sigma after a process has been established

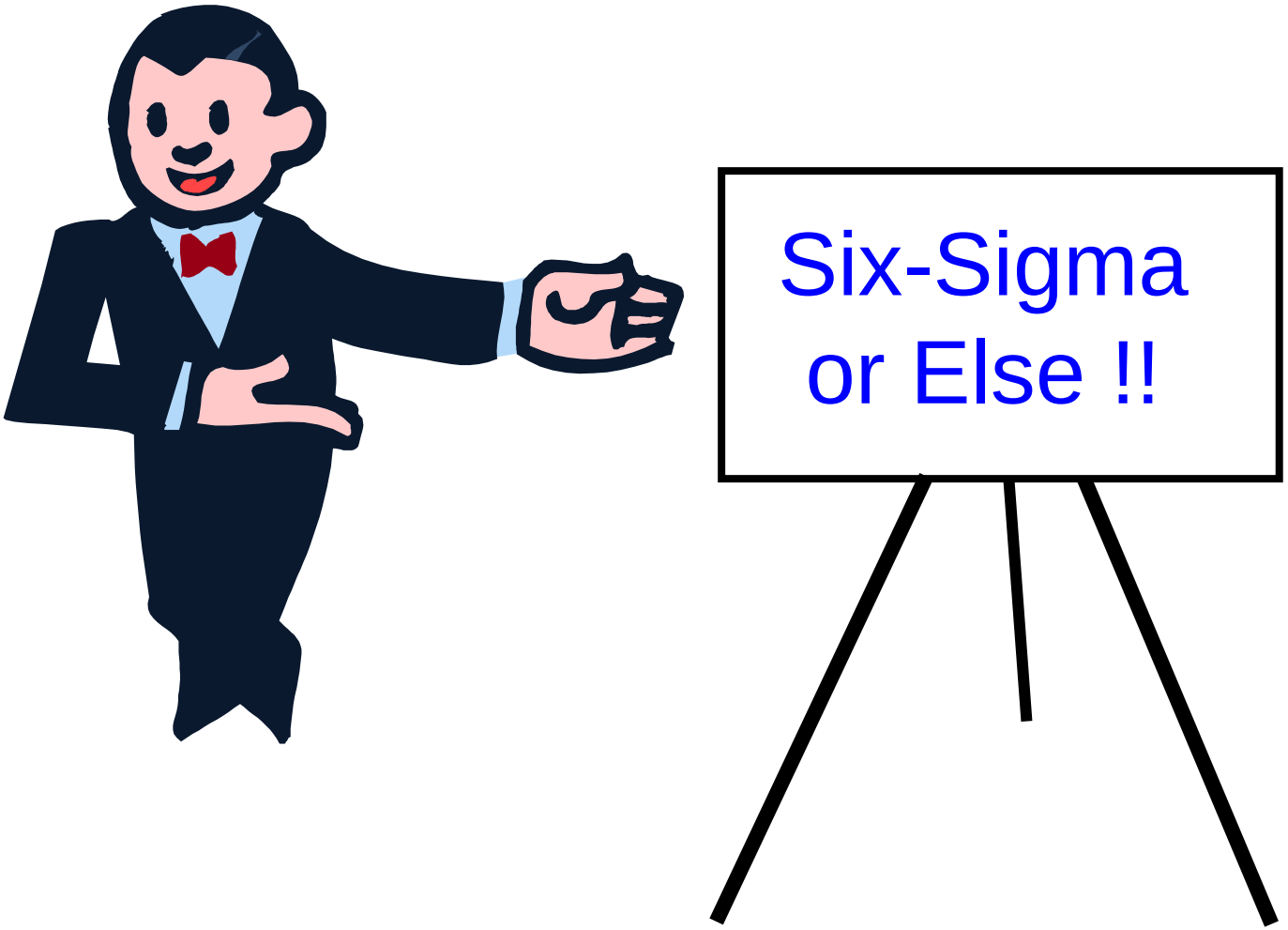
Initial "six-sigma" solutions really expect only 4.5 sigma performance in steady-state production

Assumption : Processes of interest are Gaussian (Normal)

4.5 sigma performance corresponds to 3.4 defects in a million

Observation: Any Normally distributed random variable can be mapped to a N(0,1) random variable by subtracting the mean and dividing by the variance

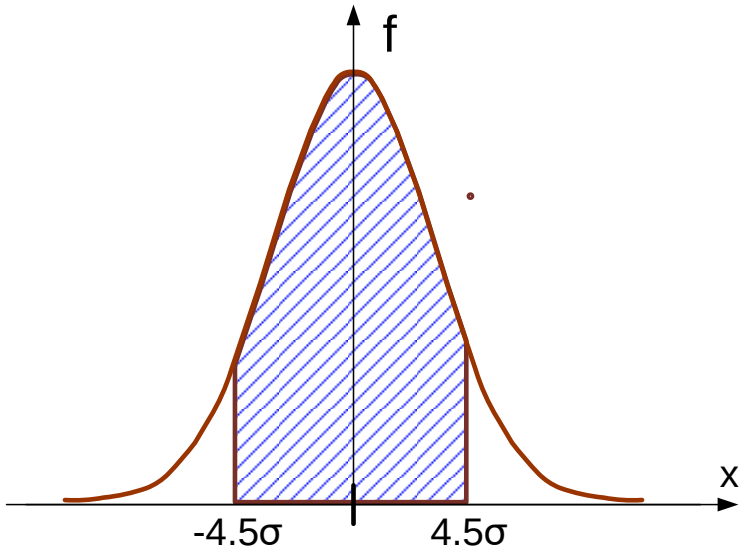
Meeting the Real Six-Sigma Challenge

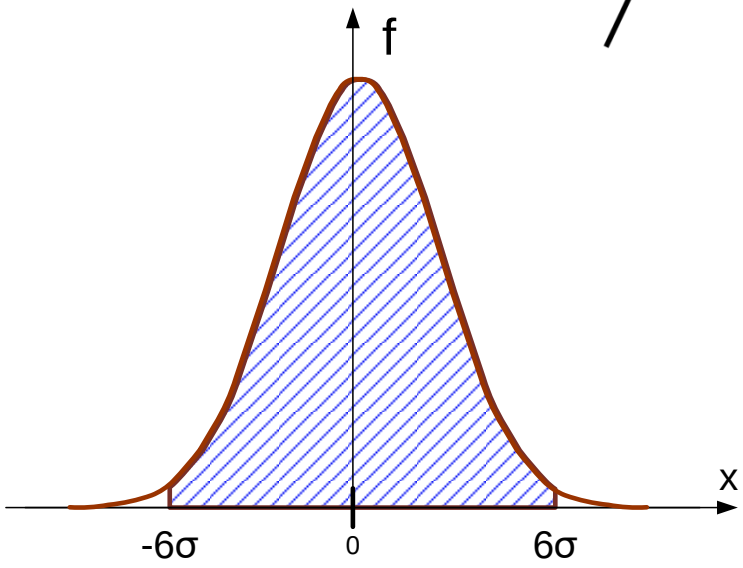


Highly Statistical Concept !

The Six-Sigma Challenge

Two-sided capability:





Long-term Capability

Tails are 6.8 parts in a million

Short-term Capability

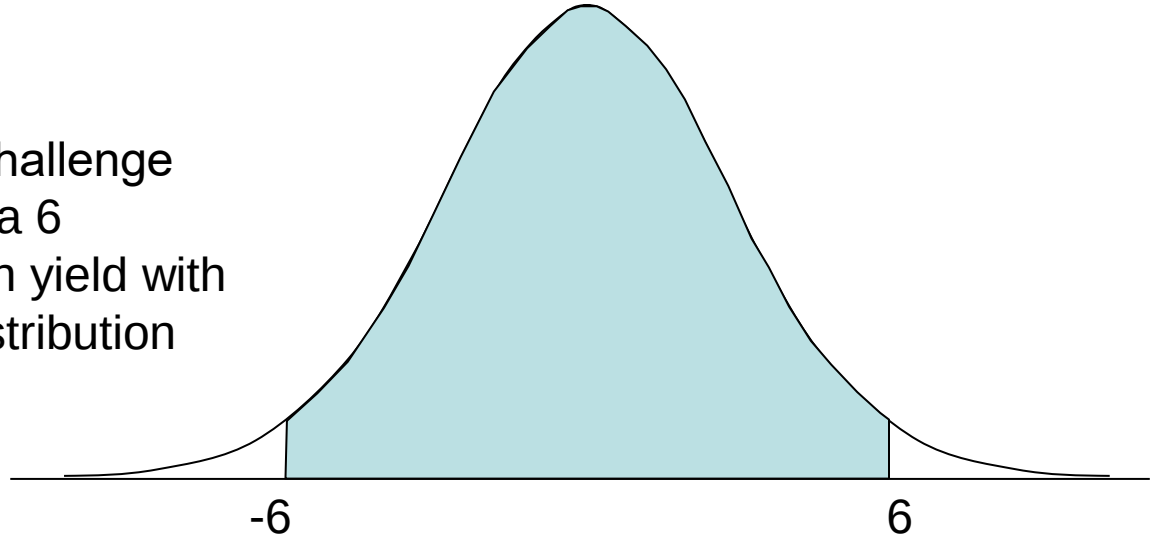
Tail is 2 parts in a billion

Six Sigma Performance is Very Good !!!

Example: Determine the maximum die area if the circuit yield is to initially meet the "six sigma" challenge for hard yield defects (Assume a defect density of $1cm^{-2}$ and only hard yield loss). Is it realistic to set six-sigma die yield expectations on the design and process engineers?

Solution:

The "six-sigma" challenge requires meeting a 6 standard deviation yield with a Normal (0,1) distribution



$$Y_{6sigma} = 2F_N(6) - 1$$

Recall: $F_N(6)=0.999999980$

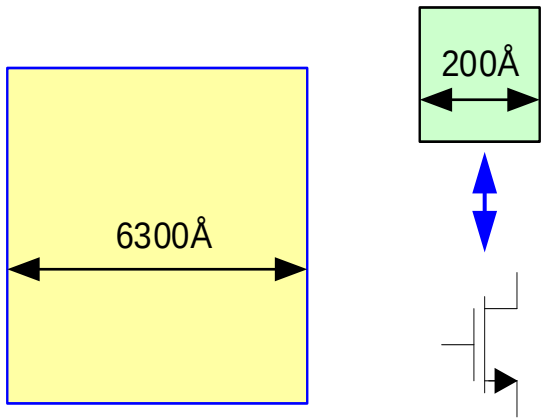
$$Y_{6sigma} = 0.999999996$$

Solution cont:

$$Y_H = e^{-Ad}$$

$$A = \frac{-\ln(Y_H)}{d}$$

$$A = \frac{-\ln(.9999999980)}{1cm^{-2}} = 4.0E-9cm^2 = 40E6(\mathring{A})^2$$



This is comparable to the area required to fabricate about 100 transistors in a state of the art 20nm process (assuming 10x overhead)

Solution cont:

Is it realistic to set six-sigma die hard yield expectations on the design and process engineers?

The best technologies in the world have orders of magnitude too many defects to build any useful integrated circuits with die yields that meet six-sigma performance requirements !!

Arbitrarily setting six-sigma design requirements will guarantee financial disaster !!

Meeting the Real Six-Sigma Challenge

Meeting the Real Six-Sigma Challenge

Improving a yield by even one sigma often is VERY challenging !!

Statistics can be abused !

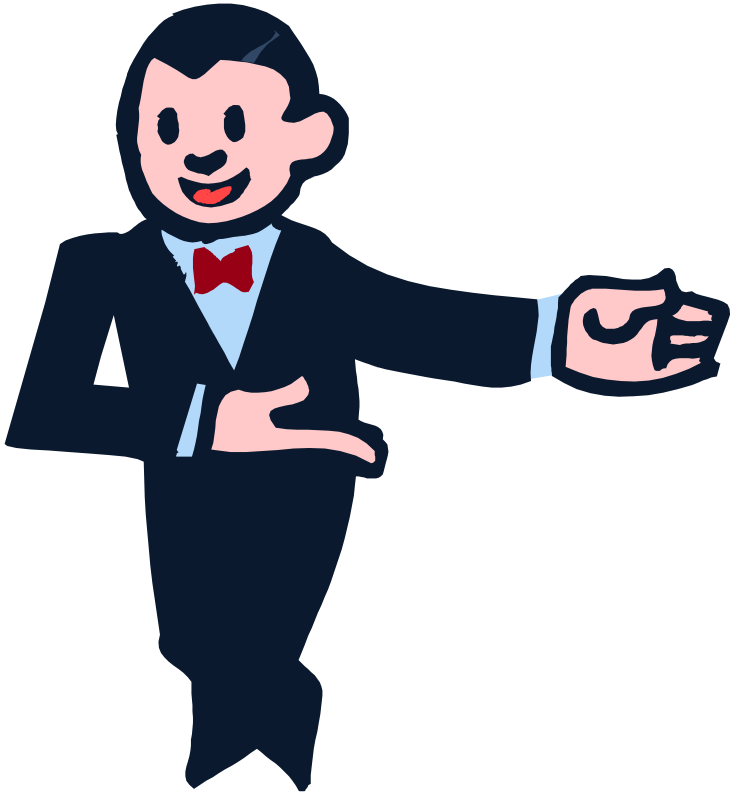
Many that are not knowledgeable incorrectly use statistics

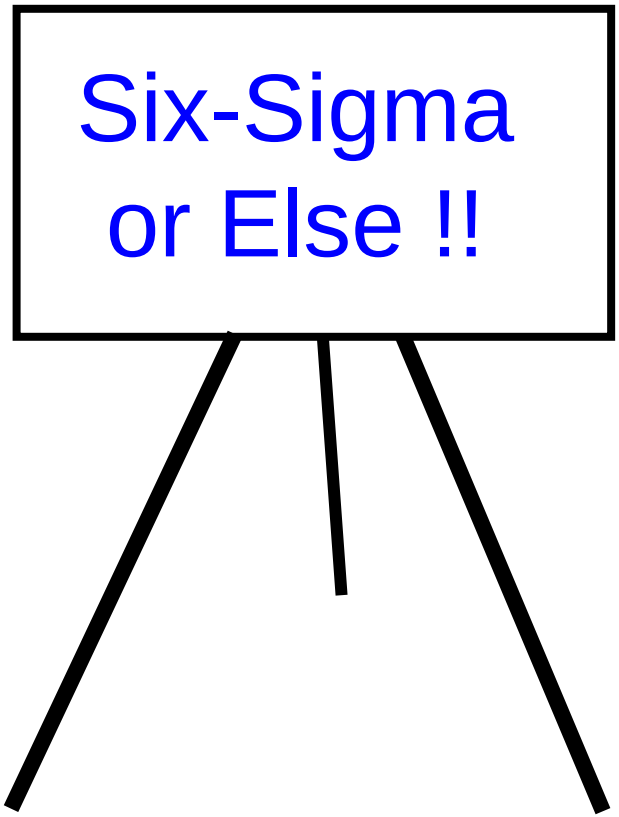
Many use statistics to intentionally mislead the public

Some openly abuse statistics for financial gain or for manipulation purposes

Keep an open mind to separate “good” statistics from “abused” statistics

Meeting the Real Six-Sigma Challenge

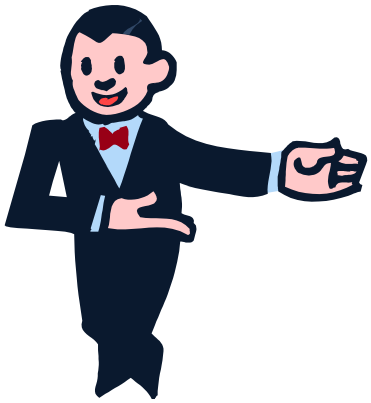




How has Motorola fared with the 6-sigma approach?

Motorola, Inc. (pronounced) was an American multinational[6] telecommunications company based in Schaumburg, Illinois, which was eventually divided into two independent public companies, Motorola Mobility and Motorola Solutions on January 4, 2011, after losing $4.3 billion from 2007 to 2009.[7]

Meeting the Real Six-Sigma Challenge



How has Motorola fared with the 6-sigma approach?

MOTOROLA

Former type	Public company
Industry	Telecommunications
Fate	Divided into Motorola Mobility and Motorola Solutions
Successor	Motorola Mobility Motorola Solutions
Founded	September 25, 1928
Defunct	January 4, 2011

- Sold military activities to General Dynamics 2000/2001
- Sold automotive products in 2006
- Spun of discrete components as ON semiconductor in 1999
- Spun of SPS as Freescale in 2003 - Acquired by NXP in 2015
- Sold Motorola Mobility to Google in 2011 – Acquired by Lonovo in 2014
- Motorola Solutions has 16,000 employees (ref fall 2018) , down from over 150,000 in mid ‘90s

The “Motorola” saga continues

Qualcomm, NXP strike $38B semiconductor deal | PitchBook
https://pitchbook.com/news/articles/qualcomm-nxp-strike-38b-semiconductor-deal
Oct 27, 2016 - **Qualcomm** has agreed to acquire **NXP** Semiconductors for $110 per ... The **deal** represents an enterprise value of $47 billion and an equity ...

Trump Blocks Broadcom's Bid for Qualcomm - The New York Times
https://www.nytimes.com/2018/03/12/.../trump-broadcom-qualcomm-merger.html
Mar 12, 2018 - Image. **Broadcom** had been trying for months to buy **Qualcomm**, and .... change the world of **mergers** and acquisitions and open the door to the ...

Will China Approve Qualcomm's NXP Acquisition? - Forbes
https://www.forbes.com/sites/.../05/.../will-china-approve-qualcomms-nxp-acquisition/
May 16, 2018 - Qualcomm's deal to purchase **NXP** Semiconductors has been caught in the crosshairs of the trade tensions between the U.S. and China, with ...

Chinese regulators approve Qualcomm purchase of NXP for US$44 ...
https://www.scmp.com › Business › Companies
Jun 15, 2018 - Chinese regulators have approved US semiconductor company Qualcomm's proposed US$44 billion **acquisition** of Dutch chip maker **NXP** ...

Qualcomm drops NXP acquisition, leaves analysts concerned about ...
https://www.marketwatch.com › Industries › The Ratings Game
Jul 26, 2018 - Nearly two years after Qualcomm Inc. announced its intent to **acquire NXP** Semiconductors NV, investors are pleased that the company is ...

Freescale Semiconductor

Semiconductor manufacturing company

Freescale Semiconductor, Inc. was an American multinational corporation headquartered in Austin, Texas, with design, research and development, manufacturing and sales operations in more than 75 locations in 19 countries. Wikipedia

Headquarters: Austin, TX

CEO: Gregg A. Lowe (Jun 2012–)

Number of employees: 17,300 (2015)

Defunct: December 7, 2015

Parent organization: Freescale Semiconductor Holdings I Ltd

Subsidiaries: Freescale Semiconductor ... an Ltd, MORE

http://www.chicagomag.com/Chicago-Magazine/September-2014/What-Happened-to-Motorola/

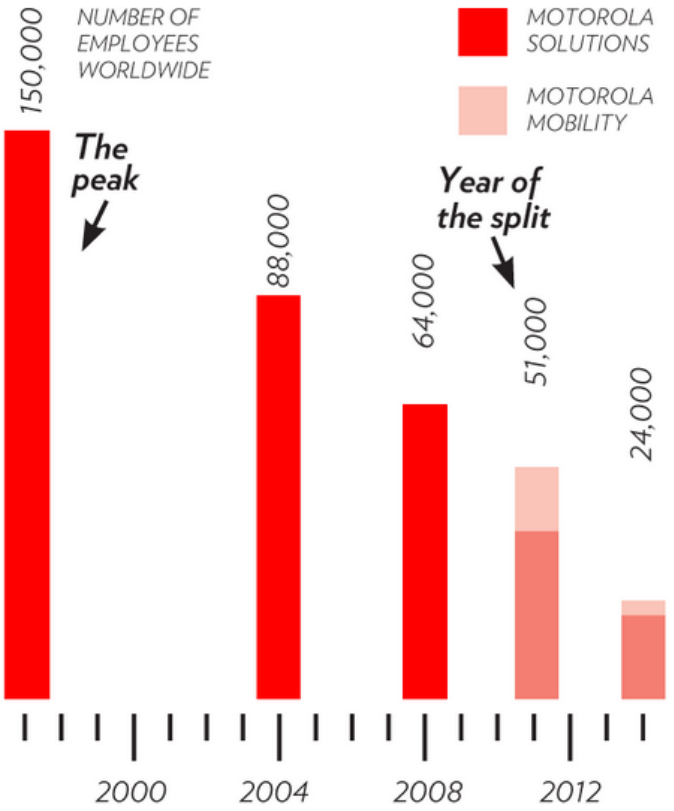
Not every important Motorola innovation during Bob's time led to a physical product. For example, in the early 1980s—a period when American companies were struggling to compete with superior products pouring out of Japan—Motorola developed a system for total quality management called Six Sigma. (A Six Sigma process is one in which 99.99966 percent of products are free from manufacturing defects.) A good chunk of the Fortune 500, including General Electric, IBM, and Boeing, wound up adopting it.

Motorola Mobility acquired by Lonovo in 2014

MOTOROLA SOLUTIONS	
Type	Public
Traded as	NYSE: MSI S&P 500 Component
Industry	Telecommunications equipment
Predecessor	Motorola, Inc.
Founded	January 4, 2011; 7 years ago
Headquarters	Chicago, Illinois, U.S.
Key people	Greg Brown (Chairman and CEO)
Products	Two-way radios, radio systems, managed services and smart public safety applications
Revenue	▲ US$6.38 billion (2017)[1]
Operating income	▲ US$1.28 billion (2017)[1]
Net income	▼ US$-155 million (2017)[1]
Total assets	▼ US$8.21 billion (2017)[1]
Total equity	US$-1.74 billion (2017)[1]
Number of employees	16,000 (2018)[2]
Subsidiaries	Airwave Solutions Avigilon
Website	www.motorolasolutions.com

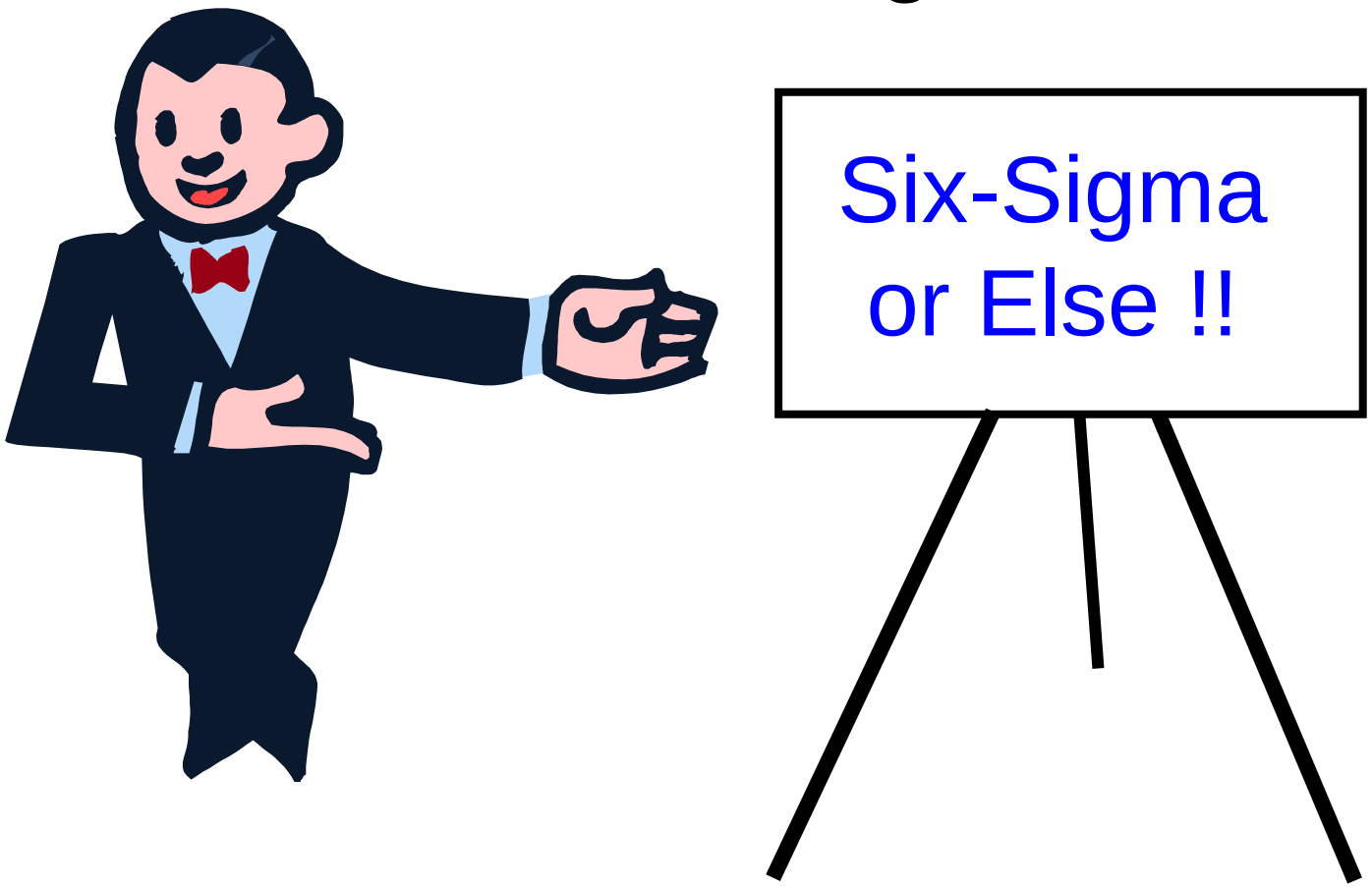
A Drastic Slimdown

In the past 17 years, Motorola and its spinoffs have reduced their total work force by 84 percent.*



NOTES: *They did so in large part by conducting layoffs and selling businesses. Motorola Solutions will shed 4,500 more jobs this fall, when Zebra Technologies completes its purchase of the company's enterprise division. Data for 2014 as of June 30.
SOURCES: Google; Motorola Solutions.

Meeting the Real Six-Sigma Challenge

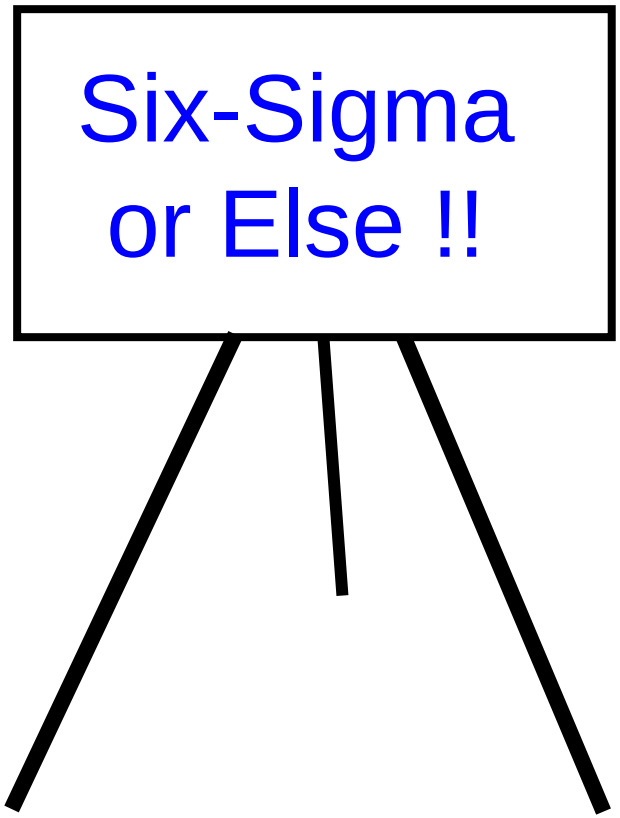


Six-sigma capability has almost nothing to do with optimizing profits and, if taken seriously, will likely guarantee a financial fiasco in most manufacturing processes

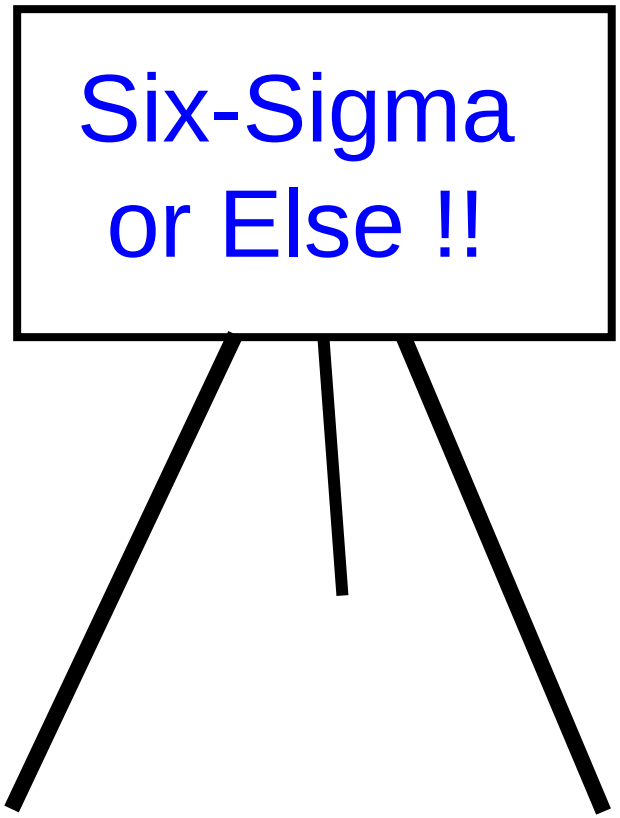
Meeting the real Six-Sigma Challenge

Six-Sigma or Else !!

Meeting the real Six-Sigma Challenge

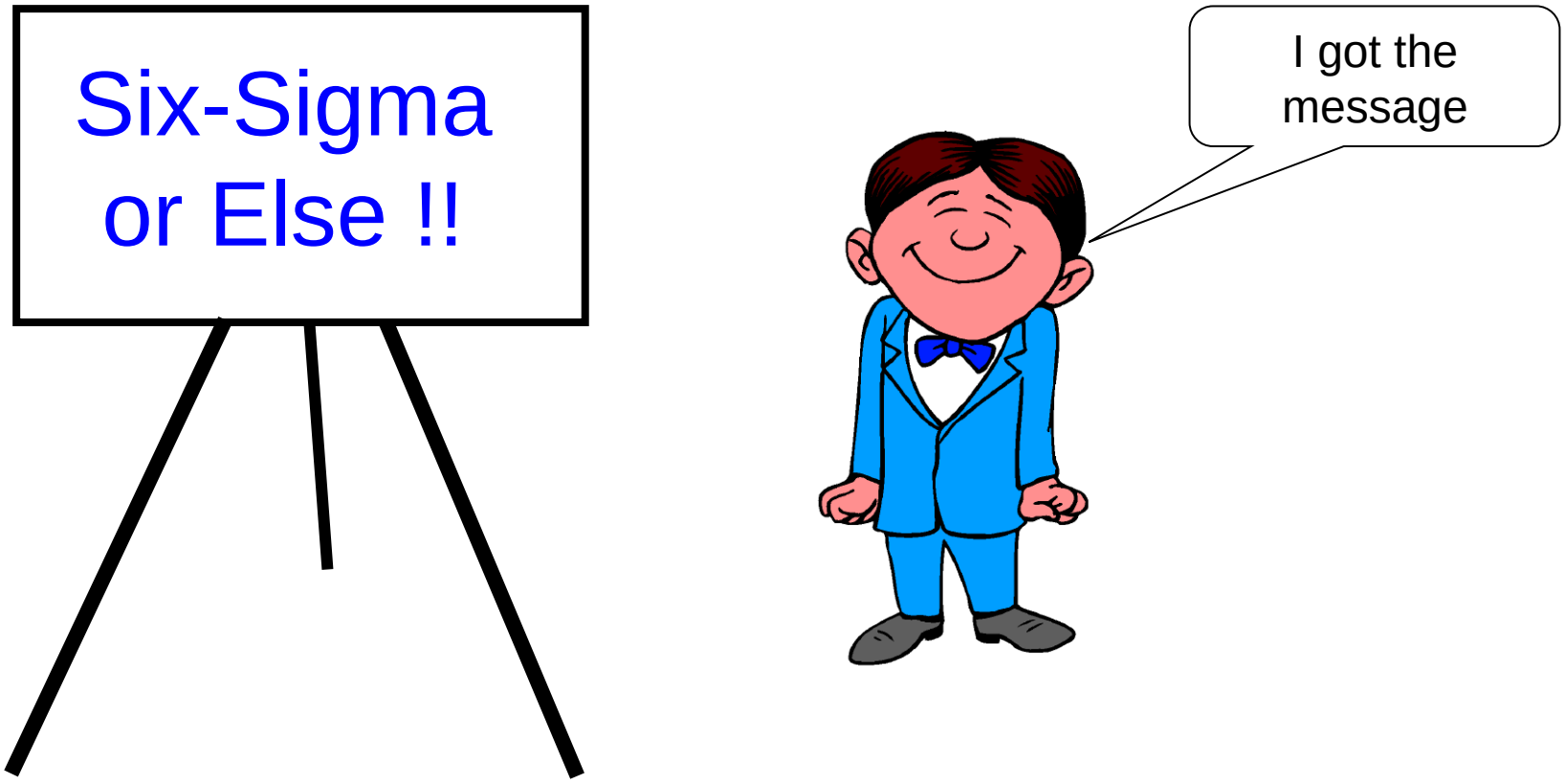


Meeting the real Six-Sigma Challenge

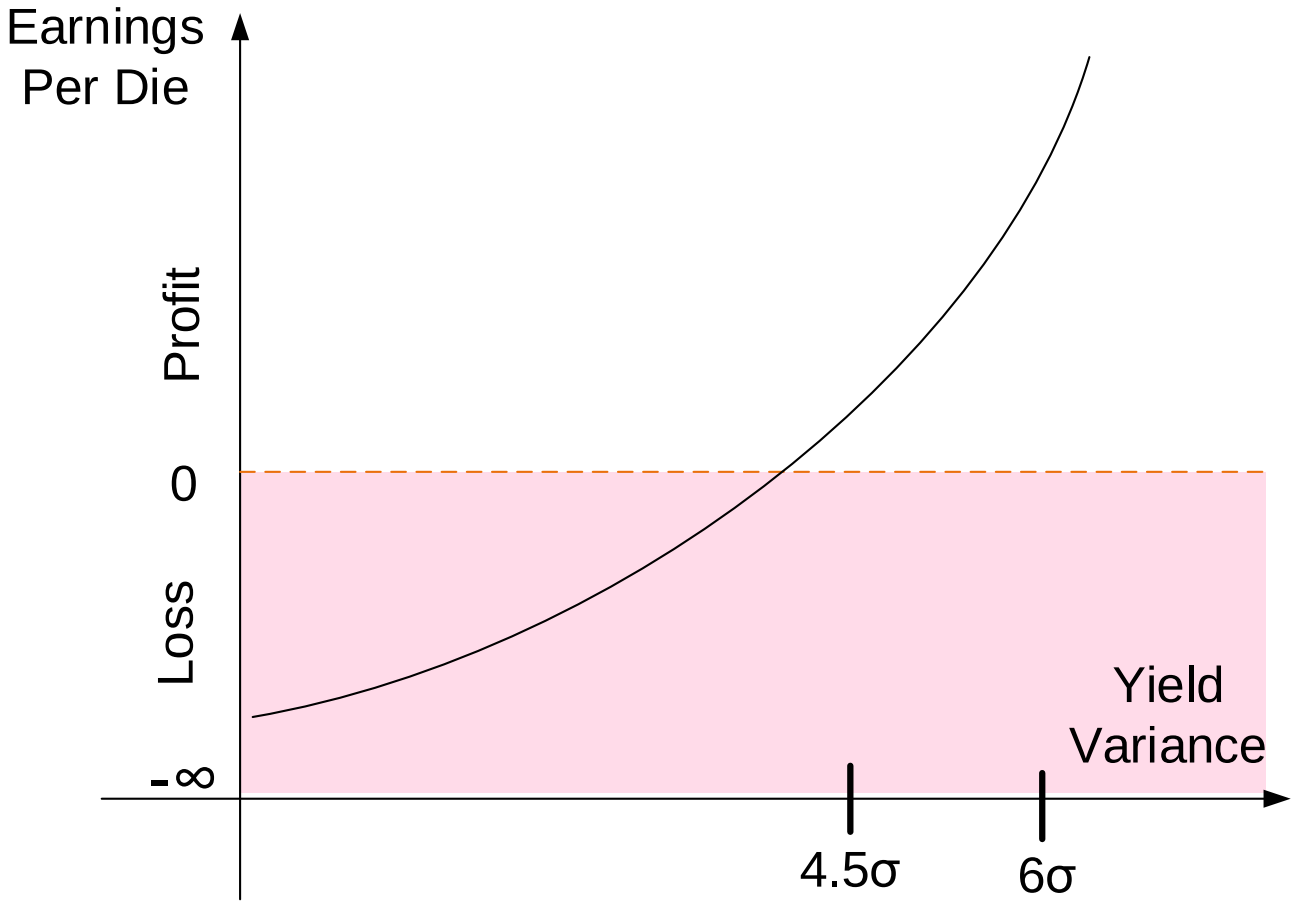


The concept of improving reliability (really profitability) is good – its just the statistics that are abused!

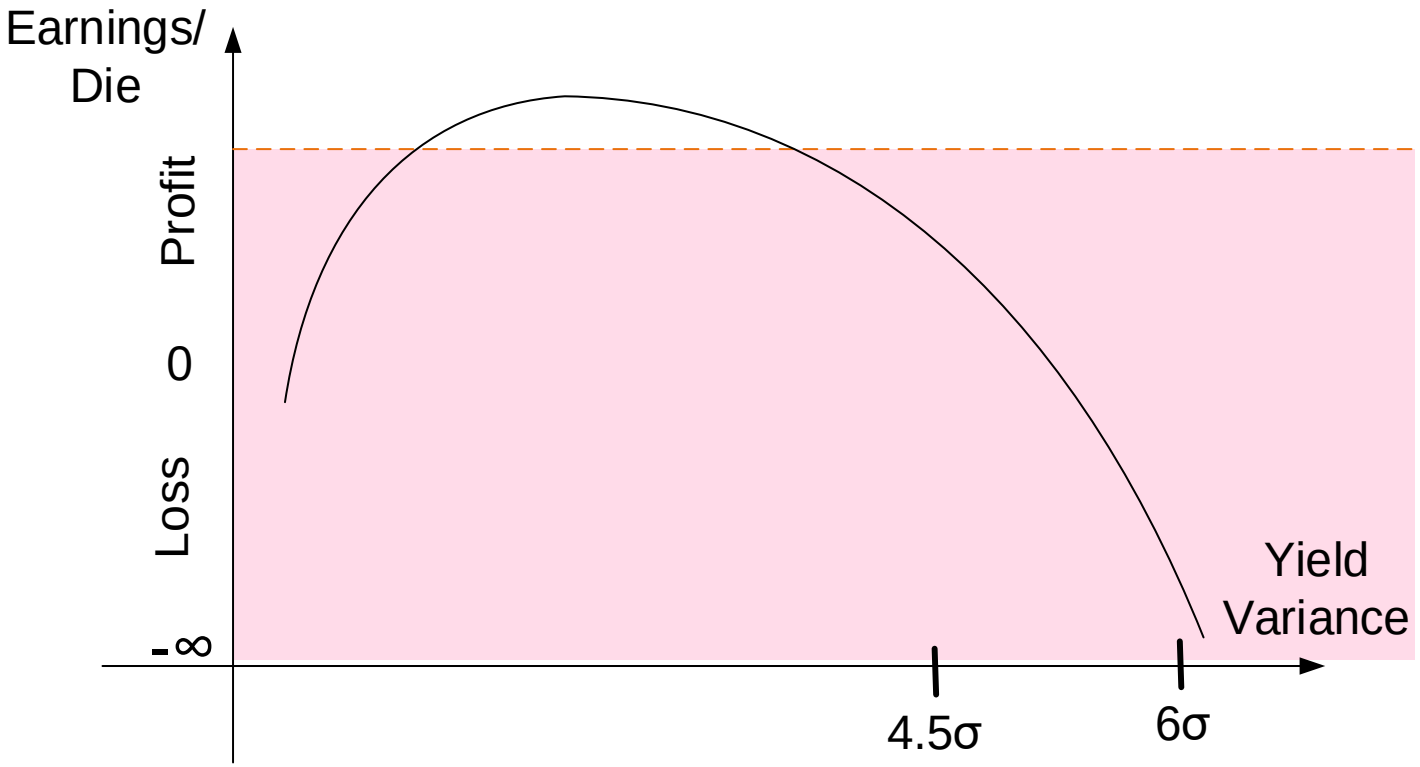
Meeting the real Six-Sigma Challenge



The Perception

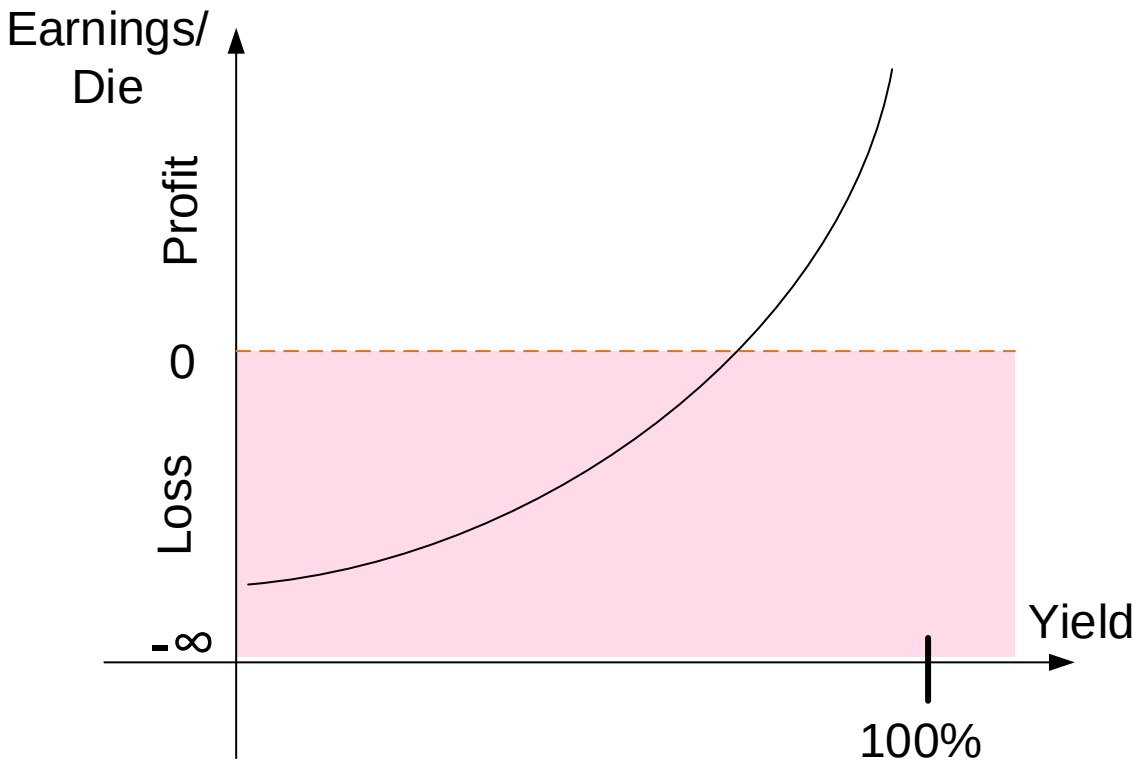


The Reality



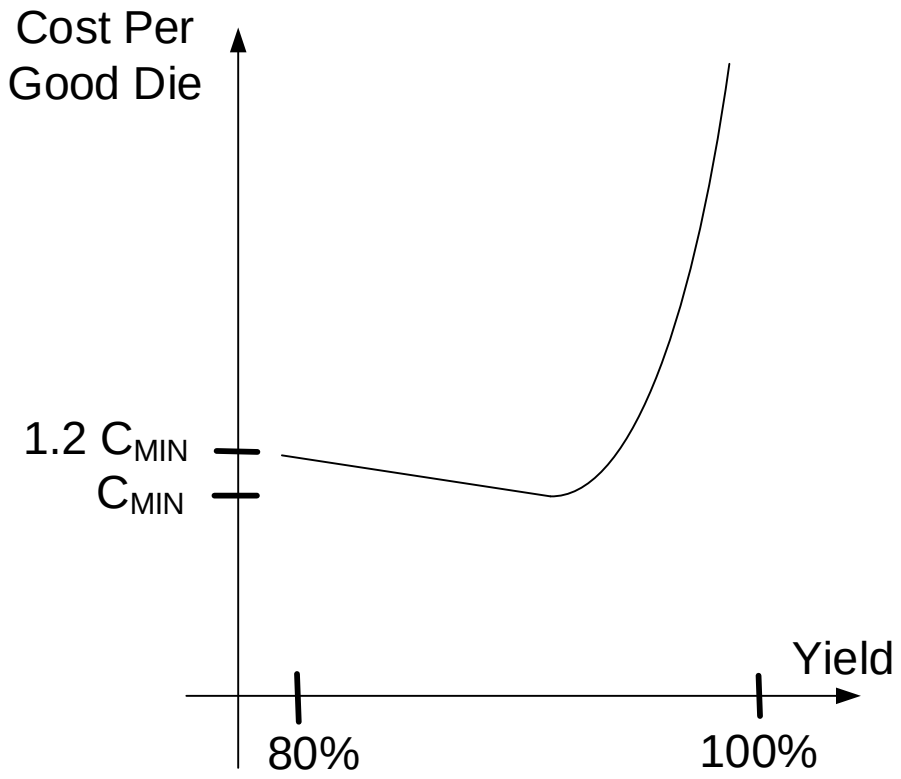
- Designing for 4.5σ or 6σ yield variance will almost always guarantee large losses
- Yield targets should be established to optimize earnings not yield variance

The Perception on Yield



Perception is often that goal should be to get yields as close to 100% as possible

The Reality about Yield



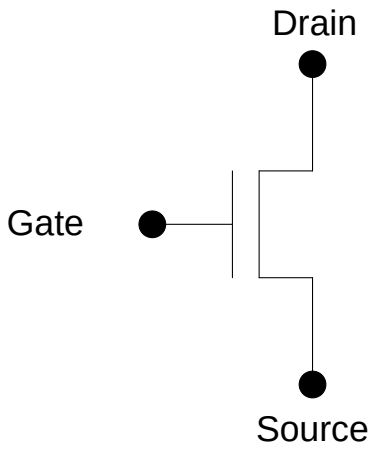
- Return on improving yield when yield is above 95% is small
- Inflection point could be at 99% or higher for some designs but below 50% for others
- Cost/good die will ultimately go to ∞ as yield approaches 100%

Designers goal should be to optimize profit, not arbitrary yield target

Key Historical Developments

- 1925,1935 Concept of MOS Transistor Proposed (Lilienfield and Heil)
- 1947 BJT Conceived and Experimentally Verified (Bardeen, Bratin and Shockley of Bell Labs)
- 1959 Jack Kilby (TI) and Bob Noyce (Fairchild) invent IC
- 1963 Wanless (Fairchild) Experimentally verifies MOS Gate

The MOS Transistor (Field Effect Transistor)



Initially an idea but little more !

1926 - Field Effect Semiconductor Device Concepts Patented

Julius Lilienfeld files a patent describing a three-electrode amplifying device based on the semiconducting properties of copper sulfide. Attempts to build such a device continue through the 1930s.

Julius E. Lilienfeld, passport photo

Polish-American physicist and inventor Julius E. Lilienfeld filed a patent in 1926, "Method and Apparatus for Controlling Electric Currents," in which he proposed a three-electrode structure using copper-sulfide semiconductor material. Today this device would be called a field-effect transistor. While working at Cambridge University in 1934, German electrical engineer and inventor Oskar Heil filed a patent on controlling current flow in a semiconductor via capacitive coupling at an electrode – essentially a field-effect transistor. Although both patents were granted, no records exist to prove that Heil or Lilienfeld actually constructed functioning devices.

Lilienfeld, J. E. "Method and apparatus for controlling electric currents," *U. S. Patent No. 1,745,175* (Filed October 8, 1926. Issued January 18, 1930).
Lilienfeld, J. E. "Device for controlling electric current," *U. S. Patent No. 1,900,018* (Filed March 28, 1928. Issued March 7, 1933).
Heil, O. "Improvements in or relating to electrical amplifiers and other control arrangements and devices," *British Patent No. 439, 457* (Filed March 5, 1935. Issued December 6, 1935).

http://www.computerhistory.org/semiconductor/timeline/1926-field.html

1935 Oskar Heil improved MOSFET

From Wilipedia:

Oskar Heil (20 March 1908, in Langwieden – 15 May 1994, San Mateo, California) was a German electrical engineer and inventor. He studied physics, chemistry, mathematics, and music at the Georg-August University of Göttingen and was awarded his PhD in 1933, for his work on molecular spectroscopy.

Lilienfeld, J. E. "Method and apparatus for controlling electric currents," *U. S. Patent No. 1,745,175* (Filed October 8, 1926. Issued January 18, 1930).
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Heil, O. "Improvements in or relating to electrical amplifiers and other control arrangements and devices," *British Patent No. 439, 457* (Filed March 5, 1935. Issued December 6, 1935).

https://www.google.com/search?q=Oskar+Heil&biw=1097&bih=568&tbm=isch&imgil=19nt7iXoiQ-X0M%253A%253B8o3VY91vkR5qnM%253Bhttp%25253A%25252F%25252Fwww.avguide.ch%25252Fmagazin%25252Flautsprecher-made-in-ticino-martin-duerrenmatt-perfektioniert-den-heil&source=iu&pf=m&fir=19nt7iXoiQ-X0M%253A%252C8o3VY91vkR5qnM%252C_&usg=__67U7QCOIp8tsrLWv8y_YzTy9c7I%3D#imgrc=dv9-icif2DsZ0M%3A&usg=__67U7QCOIp8tsrLWv8y_YzTy9c7I%3D

http://www.computerhistory.org/semiconductor/timeline/1926-field.html

Patented Jan. 28, 1930 1,745,175

UNITED STATES PATENT OFFICE

JULIUS EDGAR LILIENFELD, OF BROOKLYN, NEW YORK

METHOD AND APPARATUS FOR CONTROLLING ELECTRIC CURRENTS

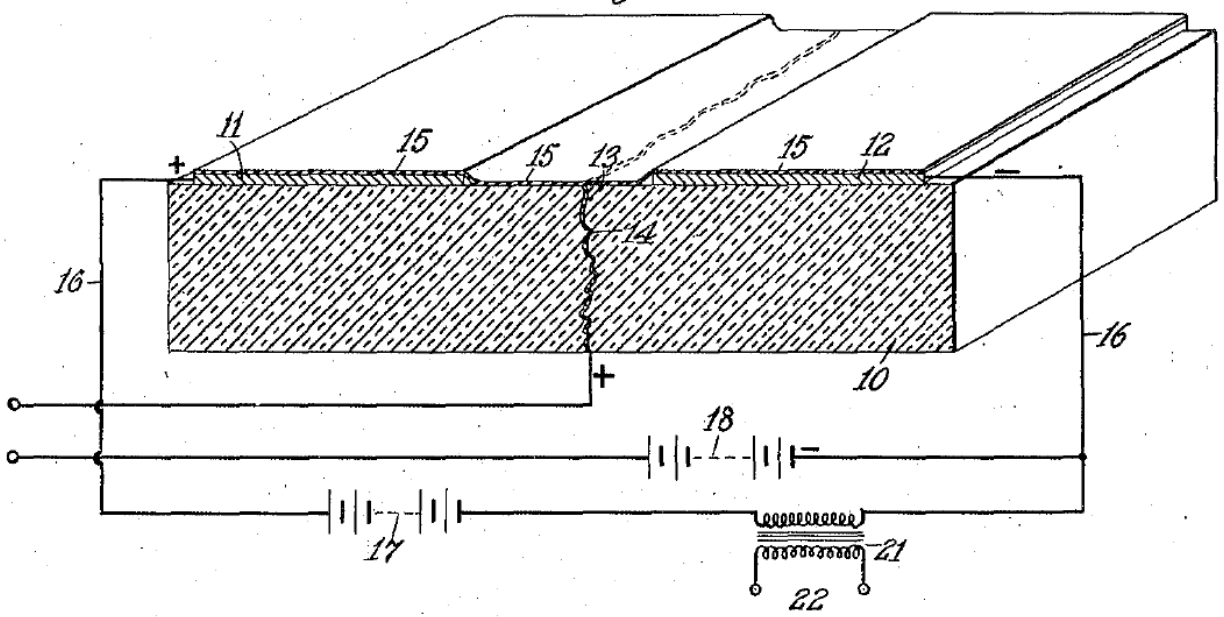
Application filed October 8, 1926, Serial No. 140,363, and in Canada October 22, 1925.

Jan. 28, 1930. J. E. LILIENFELD 1,745,175

METHOD AND APPARATUS FOR CONTROLLING ELECTRIC CURRENTS

Filed Oct. 8, 1926

Fig. 1.



March 7, 1933. J. E. LILIENFELD 1,900,018

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Filed March 28, 1928 3 Sheets-Sheet 1

Fig. 1.

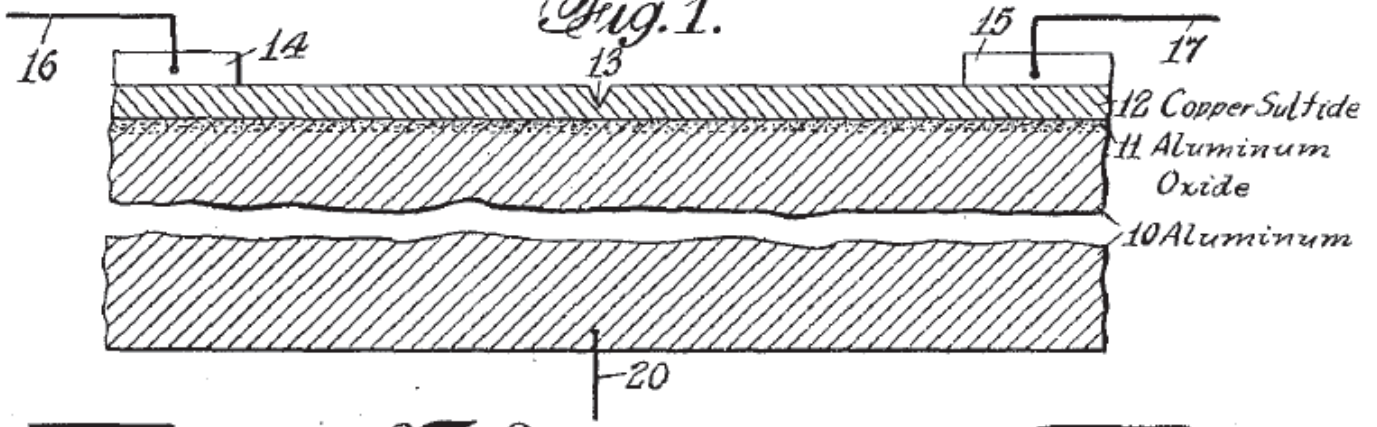
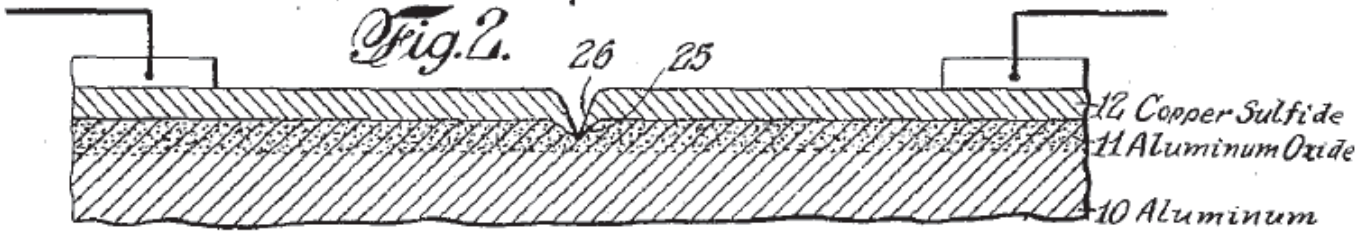


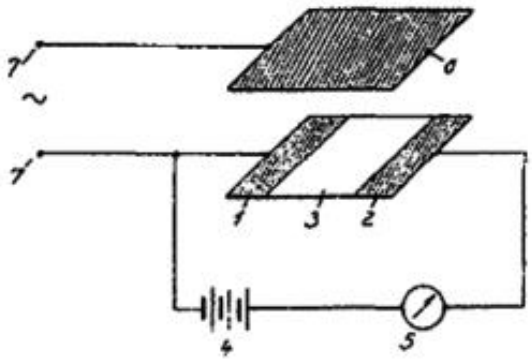
Fig. 2.



Figures from Heil 1935 patent

Insulated gate controls field between other two terminals

Fig. 1



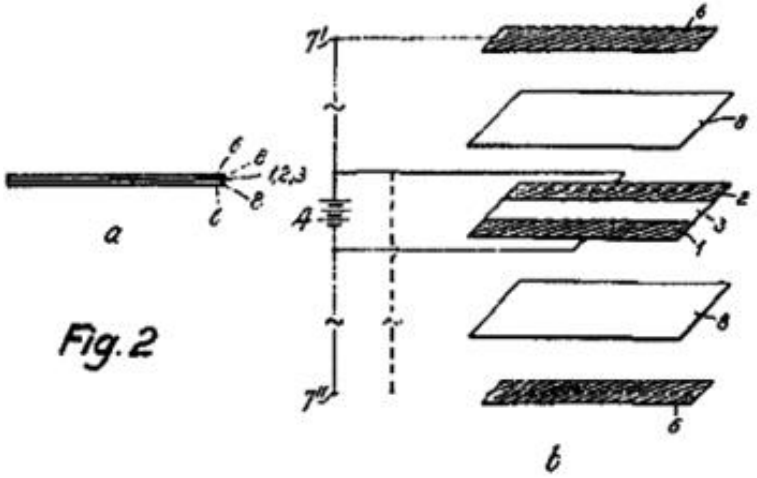


Fig. 2

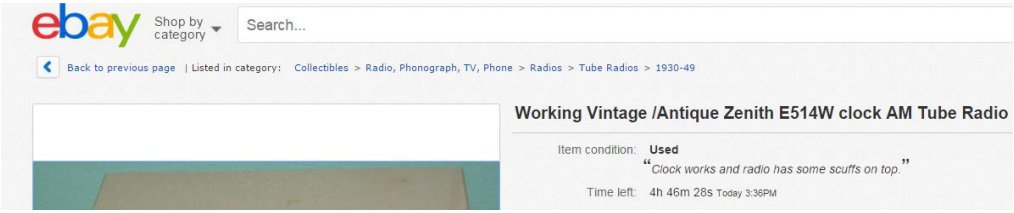
The Vacuum Tube Era

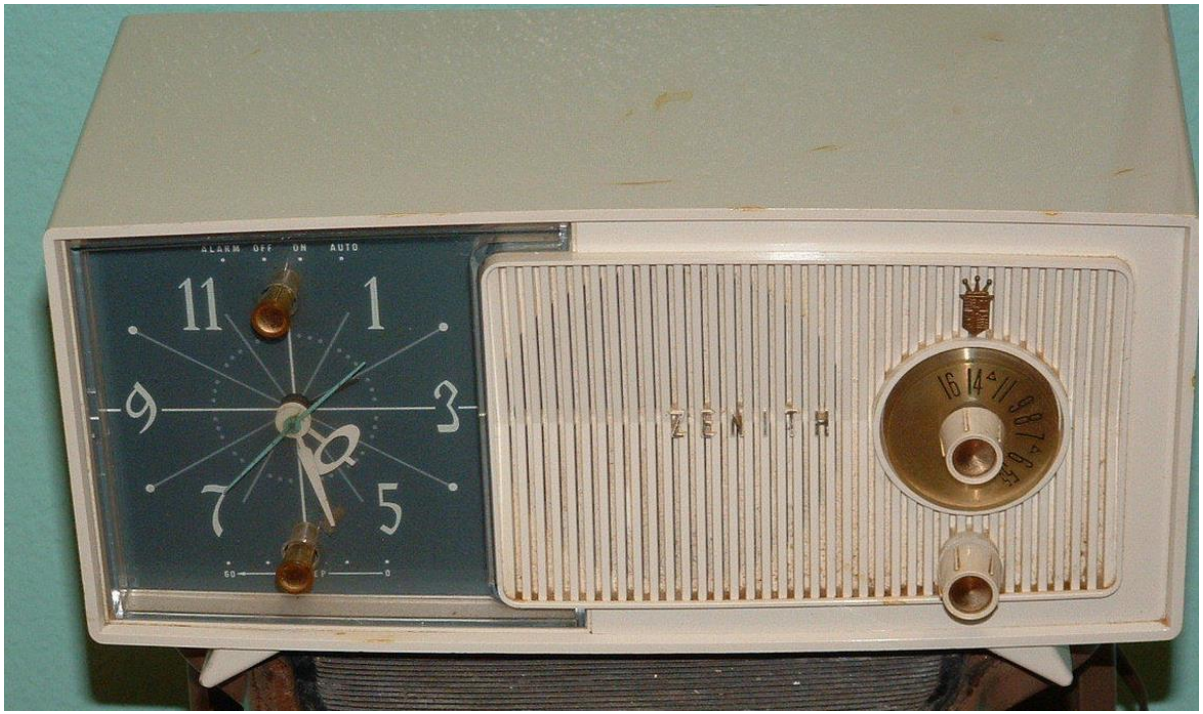
1910 to 1970

The vacuum tube (invented in 1910)

- A major breakthrough in electronics technology
- 6+ decade life span
- Vacuum tube systems not readily affordable by all of society
- Heavy, hot, expensive, large, poor reliability, fragile

The 5-Tube am radio





The 5-Tube am radio

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All American Five

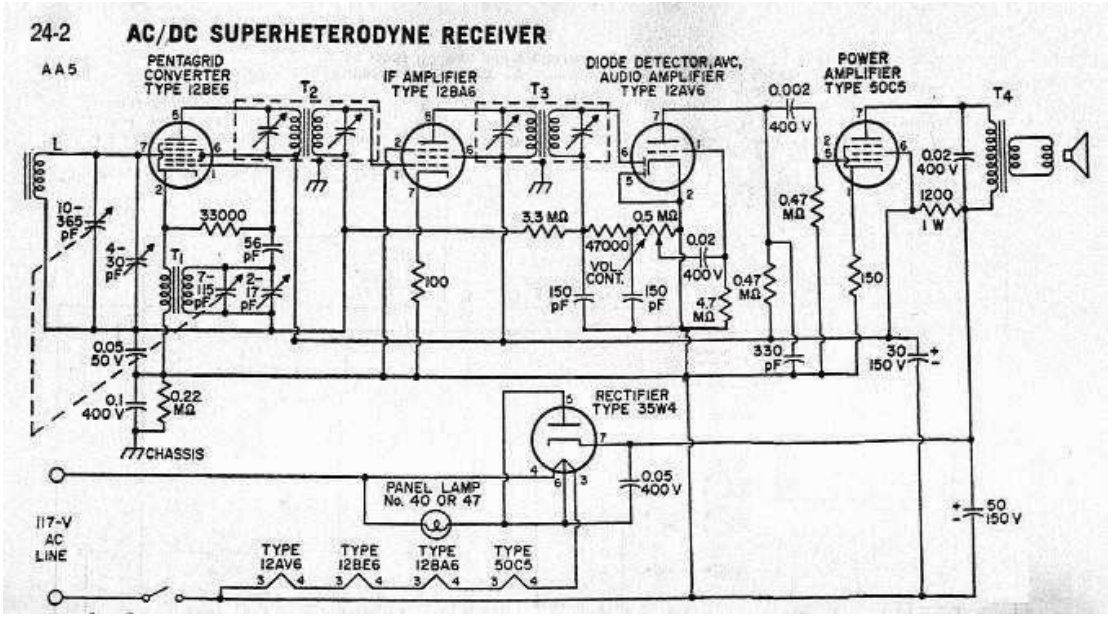
From Wikipedia, the free encyclopedia

Main page
Contents
Featured content
Current events

The term **All American Five** is a colloquial name for mass-produced, superheterodyne radio receivers that used five vacuum tubes in their design. These radio sets were designed to receive amplitude modulation (AM) broadcasts in the medium wave band, and were manufactured in the United States from the mid-1930s until the early 1960s[1] By

The 5-Tube am radio

(pictures from WEB pages of images)



Schematics were simple !!

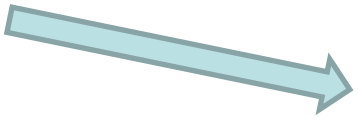
The Vacuum Tube Era

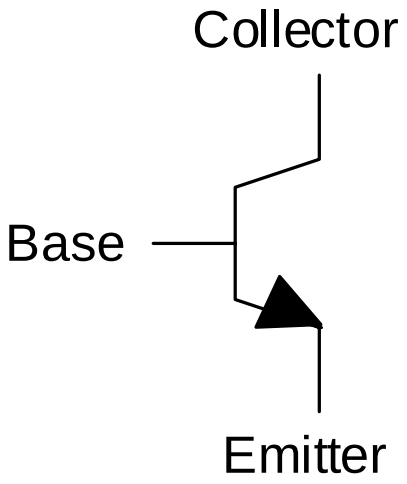
Lots of people supported the industry (primarily radio, later radio and TV) with repair shops throughout the country

(pictures from WEB pages of companies)

Tubes as well as resistors and capacitors had poor reliability

The Bipolar Transistor (Bipolar Junction Transistor – BJT)





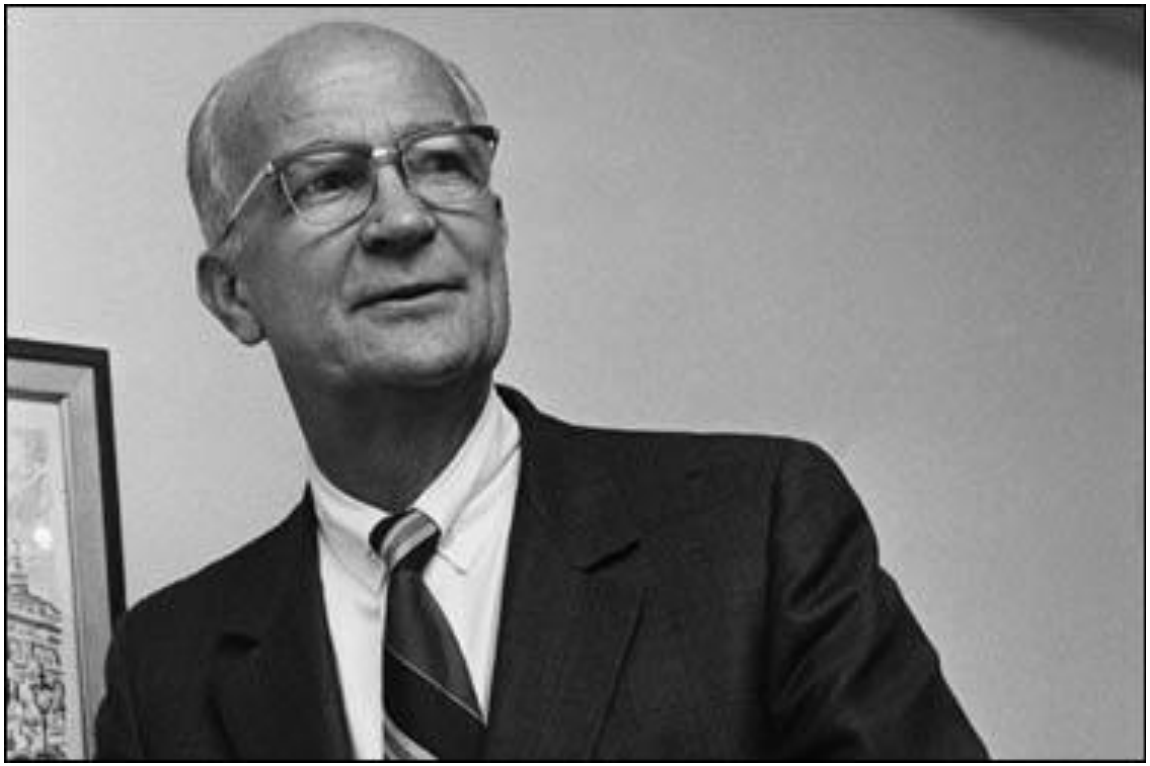
Late 1947

A solution to a major bottleneck limiting the development of electronics technology !

Naming the Transistor

From the group at Bell Labs

"We have called it the transistor, T-R-A-N-S-I-S-T-O-R, because it is resistor or semiconductor device which can amplify electrical signals as they are transferred through it from input to output terminals. It is, if you will, the electrical equivalent of a vacuum tube amplifier. But there the similarity ceases. It has no vacuum, no filament, no glass tube. It is composed entirely of cold, solid substances."



William Shockley

http://www.time.com/time/time100/scientist/profile/shockley03.html

William Shockley

He fathered the transistor and brought the silicon to Silicon Valley but is remembered by many only for his noxious racial views

By GORDON MOORE

Gordon Moore

The transistor was born just before Christmas 1947 when John Bardeen and Walter Brattain, two scientists working for William Shockley at Bell Telephone Laboratories in Murray Hill, N.J., observed that when electrical signals were applied to contacts on a crystal of germanium, the output power was larger than the input. Shockley was not present at that first observation. And though he fathered the discovery in the same way Einstein fathered the atom bomb, by advancing the idea and pointing the way, he felt left out of the momentous occasion.

Shockley, a very competitive and sometimes infuriating man, was determined to make his imprint on the discovery. He searched for an explanation of the effect from what was then known of the quantum physics of semiconductors. In a remarkable series of insights made over a few short weeks, he greatly extended the understanding of semiconductor materials and developed the underlying theory of another, much more robust amplifying device — a kind of sandwich made of a crystal with varying impurities added, which came to be known as the junction transistor. By 1951 Shockley's co-workers made his semiconductor sandwich and demonstrated that it behaved much as his theory had predicted.

Not content with his lot at Bell Labs, Shockley set out to capitalize on his invention. In doing so, he played a key role in the industrial development of the region at the base of the San Francisco Peninsula. It was Shockley who brought the silicon to Silicon Valley.

In February 1956, with financing from Beckman Instruments Inc., he founded Shockley Semiconductor Laboratory with the goal of developing and producing a silicon transistor. He chose to establish this start-up near Palo Alto, where he had grown up and where his mother still lived. He set up operations in a storefront — little more than a Quonset hut — and hired a group of young scientists (I was one of them) to develop the necessary technology. By the spring of 1956 he had a small staff in place and was beginning to undertake research and development.

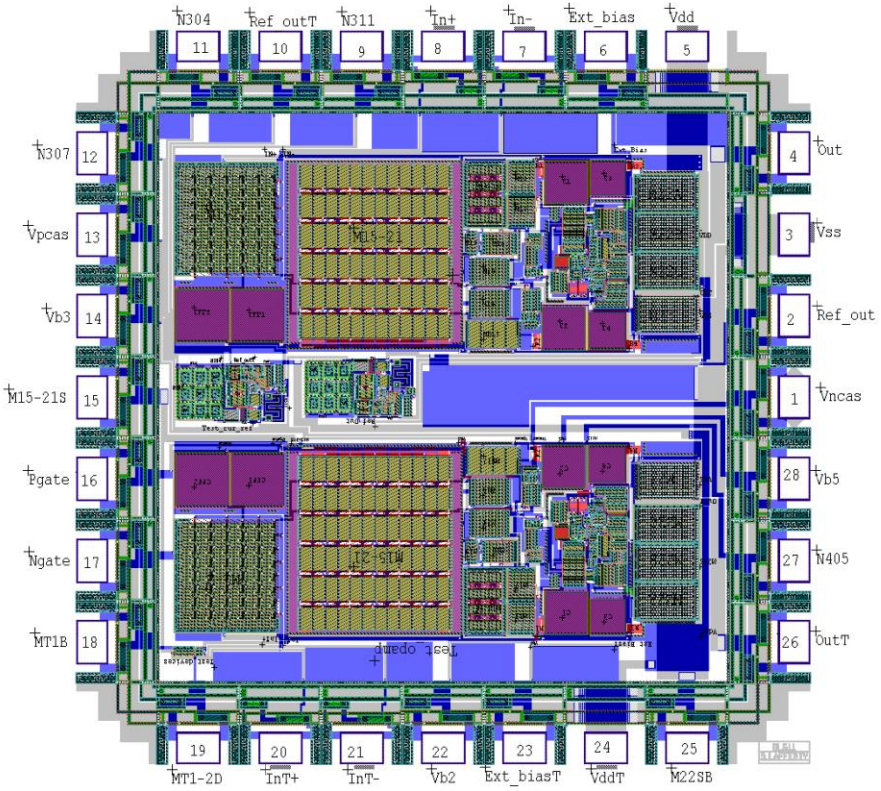
…. (in early 1957 a group of the key people involved with Shockley left and formed a new company named Fairchild Semiconductor …) This new company, financed by Fairchild Camera & Instrument Corp., became the mother organization for several dozen new companies in Silicon Valley. Nearly all the scores of companies that are or have been active in semiconductor technology can trace the technical lineage of their founders back through Fairchild to the Shockley Semiconductor Laboratory. Unintentionally, Shockley contributed to one of the most spectacular and successful industry expansions in history.

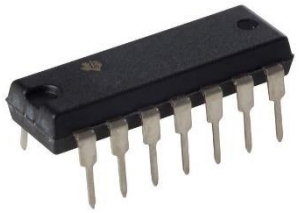
Editor's note:

In 1963 Shockley left the electronics industry and accepted an appointment at Stanford. There he became interested in the origins of human intelligence. Although he had no formal training in genetics or psychology, he began to formulate a theory of what he called dysgenics. Using data from the U.S. Army's crude pre-induction IQ tests, he concluded that African Americans were inherently less intelligent than Caucasians — an analysis that stirred wide controversy among laymen and experts in the field alike.

(Fairchild was formed in 1957 – Moore and Noyce were 2 of 8 co-founders)

The Integrated Circuit





June 23, 1964 J. S. KILBY 3,138,743

MINIATURIZED ELECTRONIC CIRCUITS

Filed Feb. 6, 1959 4 Sheets-Sheet 1

Fig. 1.

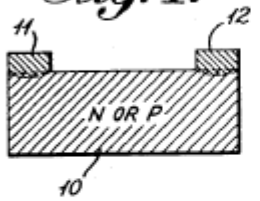


Fig. 1a.

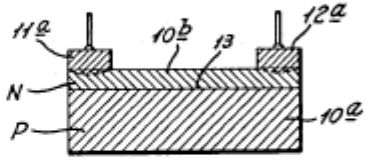


Fig. 2.

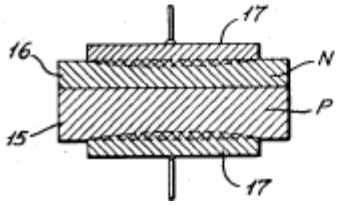


Fig. 2a.

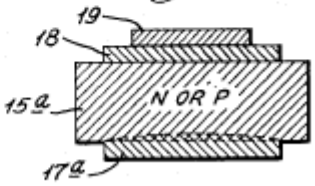


Fig. 5.

June 23, 1964 J. S. KILBY 3,138,743

MINIATURIZED ELECTRONIC CIRCUITS

Filed Feb. 6, 1959 4 Sheets-Sheet 2

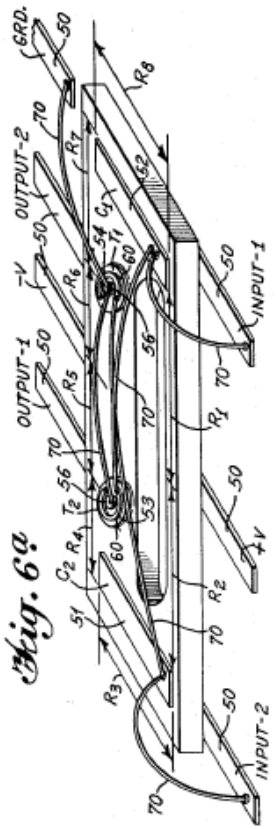


Fig. 6a.

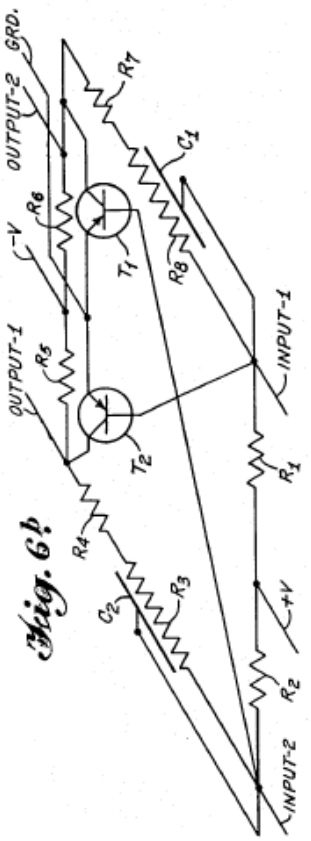


Fig. 6b.

INVENTOR

Jack S. Kilby

BY Stevens, Davis, Miller & Mosher

ATTORNEYS

United States Patent BEST AVAILABLE COPY [15] 3,643,138
Kilby [45] **Feb. 15, 1972**

[54] SEMICONDUCTOR DEVICE

[72] Inventor: **Jack St. Clair Kilby**, Dallas, Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[22] Filed: **Jan. 29, 1962**

[21] Appl. No.: **169,557**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 791,602, Feb. 6, 1959, Pat. No. 3,138,743, and a continuation-in-part of 811,476, May 6, 1959, abandoned, and a continuation-in-part of 811,486, May 6, 1959, Pat. No. 3,138,744.

[52] **U.S. Cl.** **317/235**, 317/234, 317/101
[51] **Int. Cl.** **H01l 19/00**
[58] **Field of Search** 317/234, 235, 101, 231

[56] **References Cited**

UNITED STATES PATENTS

2,680,220	6/1954	Starr et al.	317/235
2,709,232	5/1955	Thedieck	317/235
2,792,538	5/1957	Pfann	317/235
2,796,562	6/1957	Ellis et al.	317/234
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2,910,634	10/1959	Rutz	317/235
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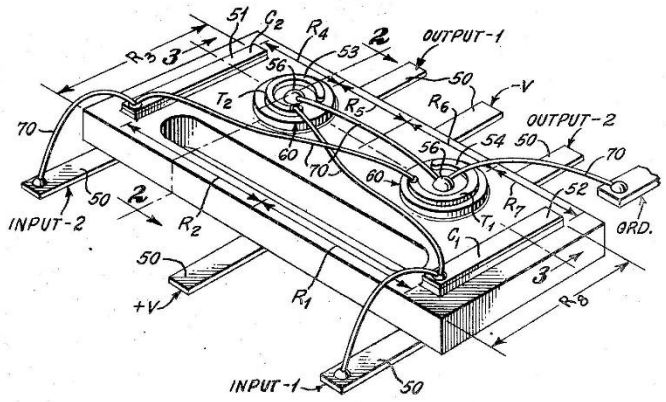
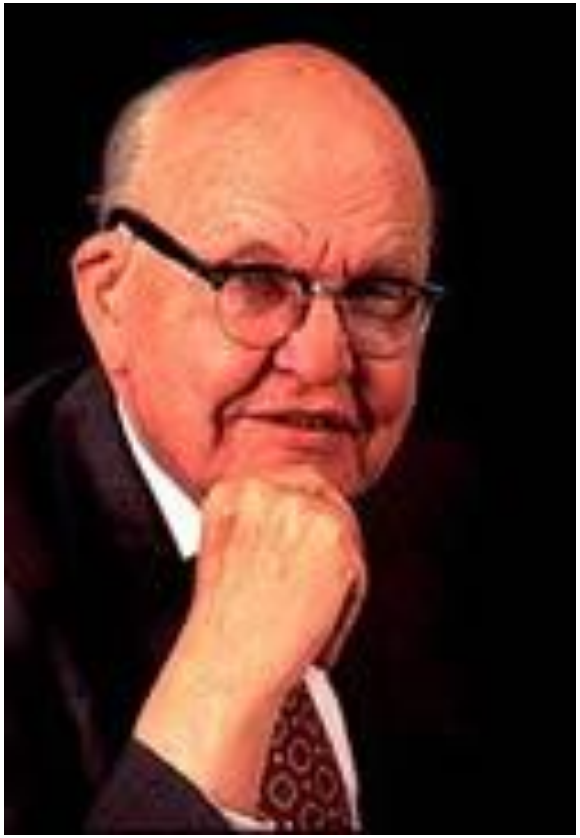
Primary Examiner—James D. Kallam
Attorney—James O. Dixon, Andrew M. Hassell, Robert C. Peterson and Stevens, Davis, Miller and Mosher

EXEMPLARY CLAIM

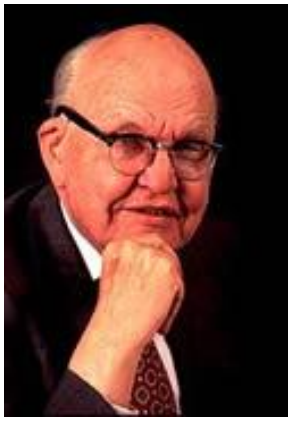
1. A semiconductor device comprising:
   a. a wafer of semiconductor material having two major faces;
   b. said wafer being so shaped as to define a plurality of regions within said wafer and adjacent to one of said major faces;
   c. at least some of said regions being electrically isolated within said wafer from others of said regions;
   d. said regions having at least one portion thereof extending to said one major face;
   e. at least some of said portions having selected locations on said one major face for electrical contact to said region;
   f. an insulating material on said one major face of the wafer excluding at least said selected locations;
   g. at least one electrically conductive area in contact with said insulating material and spaced from said wafer thereby;
   h. said electrically conductive area being disposed in cooperative relationship with respect to a selected one of said isolated regions so as to provide the electrical function of a discrete electrical circuit component: and
   i. a plurality of metallic interconnections providing electrically conductive paths between said selected locations on different ones of said regions and between another selected one of said locations and said electrically conductive area.

4 Claims, 33 Drawing Figures

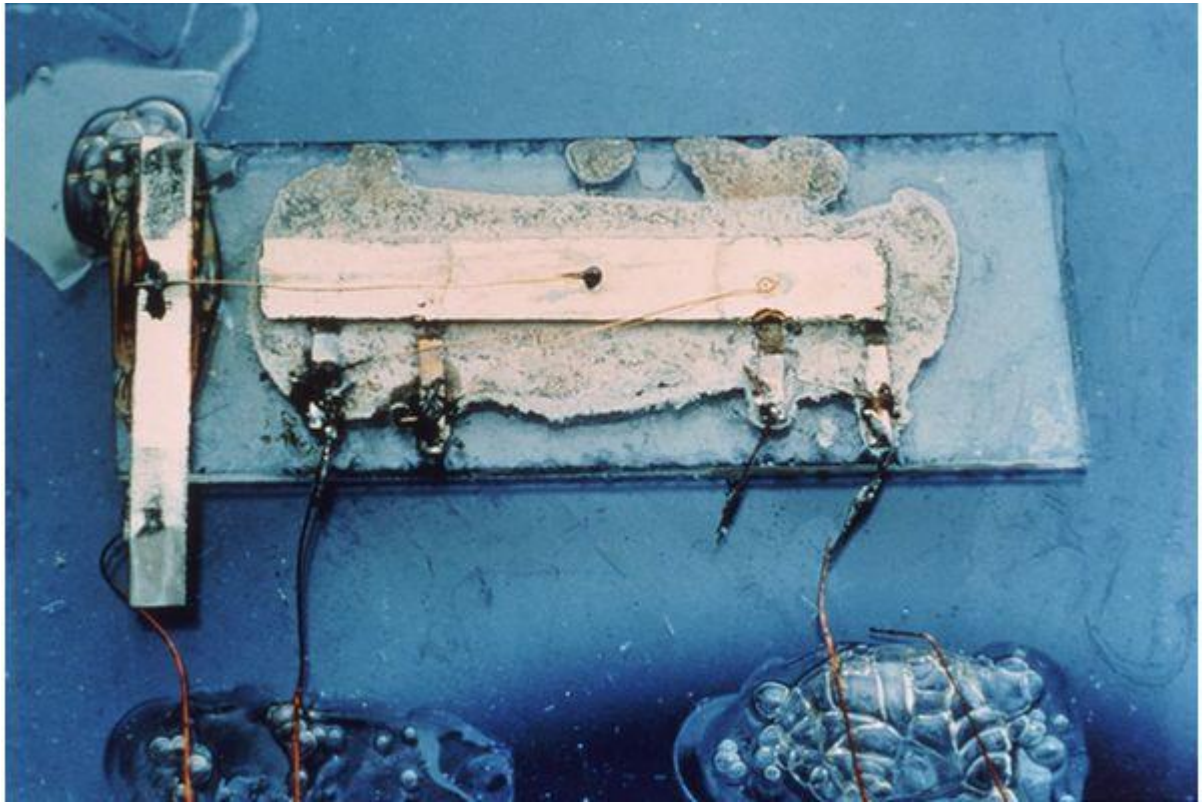




Jack Kilby



Jack Kilby



Kilby’s Integrated Circuit (germanium)

http://www.ti.com/corp/docs/kilbyctr/jackstclair.shtml

There are few men whose insights and professional accomplishments have changed the world. Jack Kilby is one of these men. His invention of the monolithic integrated circuit - the microchip - some 45 years ago at Texas Instruments (TI) laid the conceptual and technical foundation for the entire field of modern microelectronics. It was this breakthrough that made possible the sophisticated high-speed computers and large-capacity semiconductor memories of today's information age.

Mr. Kilby grew up in Great Bend, Kansas. With B.S. and M.S. degrees in electrical engineering from the Universities of Illinois and Wisconsin respectively, he began his career in 1947 with the Centralab Division of Globe Union Inc. in Milwaukee, developing ceramic-base, silk-screen circuits for consumer electronic products.

In 1958, he joined TI in Dallas. During the summer of that year working with borrowed and improvised equipment, he conceived and built the first electronic circuit in which all of the components, both active and passive, were fabricated in a single piece of semiconductor material half the size of a paper clip. The successful laboratory demonstration of that first simple microchip on September 12, 1958, made history.

Jack Kilby went on to pioneer military, industrial, and commercial applications of microchip technology. He headed teams that built both the first military system and the first computer incorporating integrated circuits. He later co-invented both the hand-held calculator and the thermal printer that was used in portable data terminals.

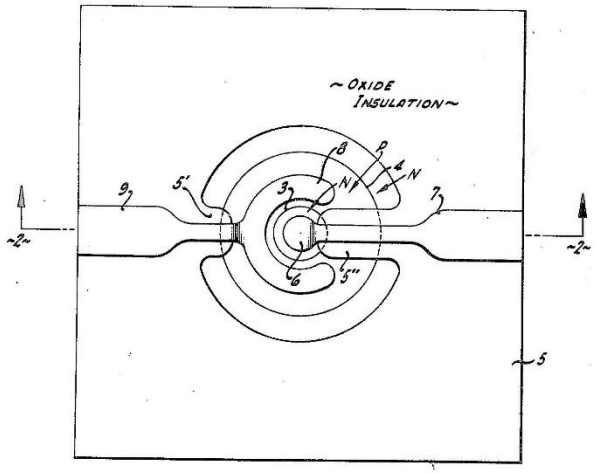
April 25, 1961 R. N. NOYCE 2,981,877

SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE

Filed July 30, 1959

3 Sheets-Sheet 1

FIG-1



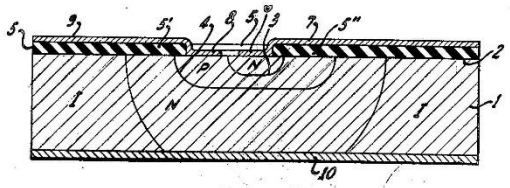
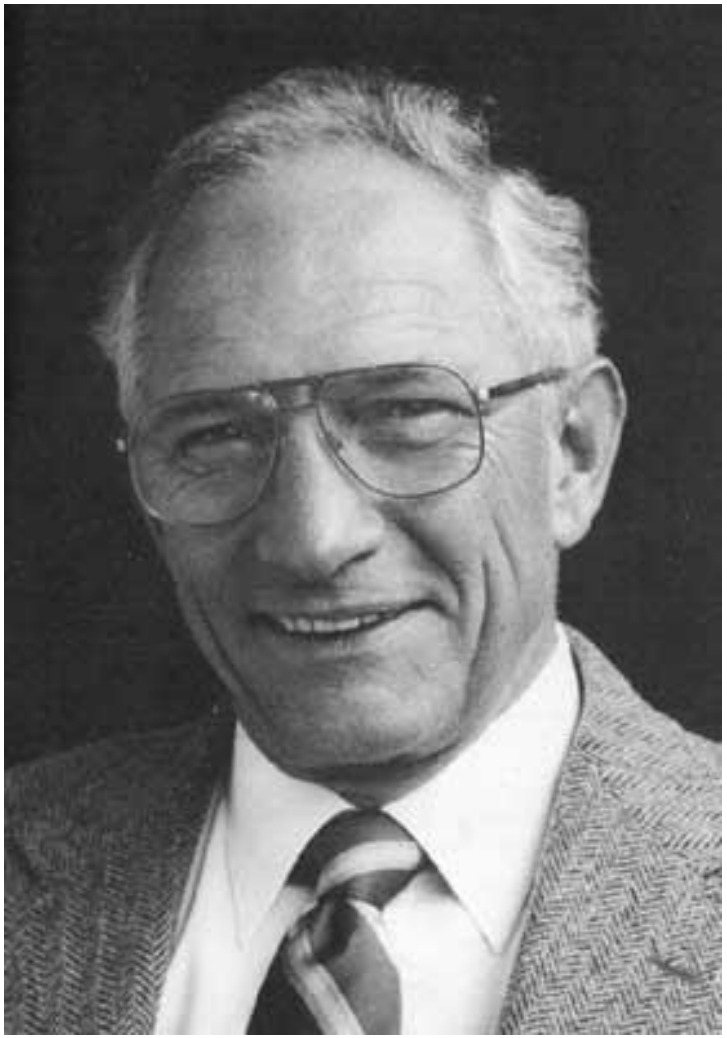


FIG-2

INVENTOR.
ROBERT N. NOYCE
BY Lieffenstett & Ralls
ATTORNEYS



Robert Noyce

http://www.ideafinder.com/history/inventors/noyce.htm

Robert Norton Noyce was born December 12, 1927 in Burlington, Iowa. A noted visionary and natural leader, Robert Noyce helped to create a new industry when he developed the technology that would eventually become the microchip. Noted as one of the original computer entrepreneurs, he founded two companies that would largely shape today's computer industry—Fairchild Semiconductor and Intel.

Bob Noyce's nickname was the "Mayor of Silicon Valley." He was one of the very first scientists to work in the area -- long before the stretch of California had earned the Silicon name -- and he ran two of the companies that had the greatest impact on the silicon industry: Fairchild Semiconductor and Intel. He also invented the integrated chip, one of the stepping stones along the way to the microprocessors in today's computers.

Noyce, the son of a preacher, grew up in Grinnell, Iowa. He was a physics major at Grinnell College, and exhibited while there an almost baffling amount of confidence. He was always the leader of the crowd. This could turn against him occasionally -- the local farmers didn't approve of him and weren't likely to forgive quickly when he did something like steal a pig for a college luau. The prank nearly got Noyce expelled, even though the only reason the farmer knew about it was because Noyce had confessed and offered to pay for it.

While in college, Noyce's physics professor Grant Gale got hold of two of the very first transistors ever to come out of Bell Labs. Gale showed them off to his class and Noyce was hooked. The field was young, though, so when Noyce went to MIT in 1948 for his Ph.D., he found he knew more about transistors than many of his professors.

After a brief stint making transistors for the electronics firm Philco, Noyce decided he wanted to work at Shockley Semiconductor. In a single day, he flew with his wife and two kids to California, bought a house, and went to visit Shockley to ask for a job -- in that order.

As it was, Shockley and Noyce's scientific vision -- and egos -- clashed. When seven of the young researchers at Shockley semiconductor got together to consider leaving the company, they realized they needed a leader. All seven thought Noyce, aged 29 but full of confidence, was the natural choice. So Noyce became the eighth in the group that left Shockley in 1957 and founded Fairchild Semiconductor.

Noyce was the general manager of the company and while there invented the integrated chip -- a chip of silicon with many transistors all etched into it at once. Fairchild Semiconductor filed a patent for a semiconductor integrated circuit based on the planar process on July 30, 1959. That was the first time he revolutionized the semiconductor industry. He stayed with Fairchild until 1968, when he left with Gordon Moore to found Intel.

At Intel he oversaw Ted Hoff's invention of the microprocessor -- that was his second revolution.

At both companies, Noyce introduced a very casual working atmosphere, the kind of atmosphere that has become a cultural stereotype of how California companies work. But along with that open atmosphere came responsibility. Noyce learned from Shockley's mistakes and he gave his young, bright employees phenomenal room to accomplish what they wished, in many ways defining the Silicon Valley working style was his third revolution.

The key patents that revolutionized the electronics field:

Jack Kilby (34 years old at invention) patent: 3,138,743

Filed Feb 6, 1959 Issued June 23, 1964

Robert Noyce (31 years old at invention) patent: 2,981,877

Filed July 30, 1959 Issued April 25, 1961

Key Historical Developments

- 1971 Intel Introduces 4004 microprocessor (2300 transistors, 10u process)

Silicon Gate MOS **4004**

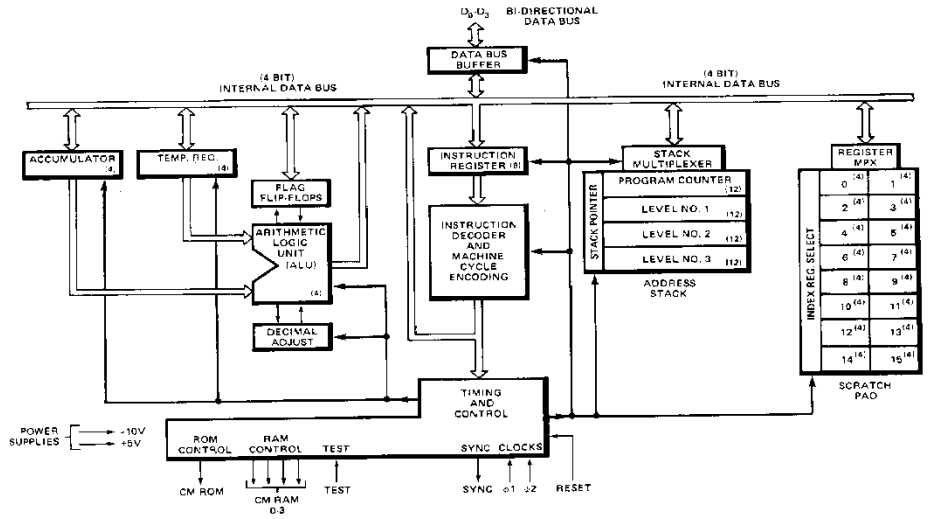
SINGLE CHIP 4-BIT P-CHANNEL MICROPROCESSOR

- **10.8 Microsecond Instruction Cycle**
- **CPU Directly Compatible With MCS-4 ROMs and RAMs**
- **Easy Expansion—One CPU can Directly Drive up to 32,768 Bits of ROM and up to 5120 Bits of RAM**
- **4-Bit Parallel CPU With 46 Instructions**
- **Instruction Set Includes Conditional Branching, Jump to Subroutine and Indirect Fetching**
- **Binary and Decimal Arithmetic Modes**

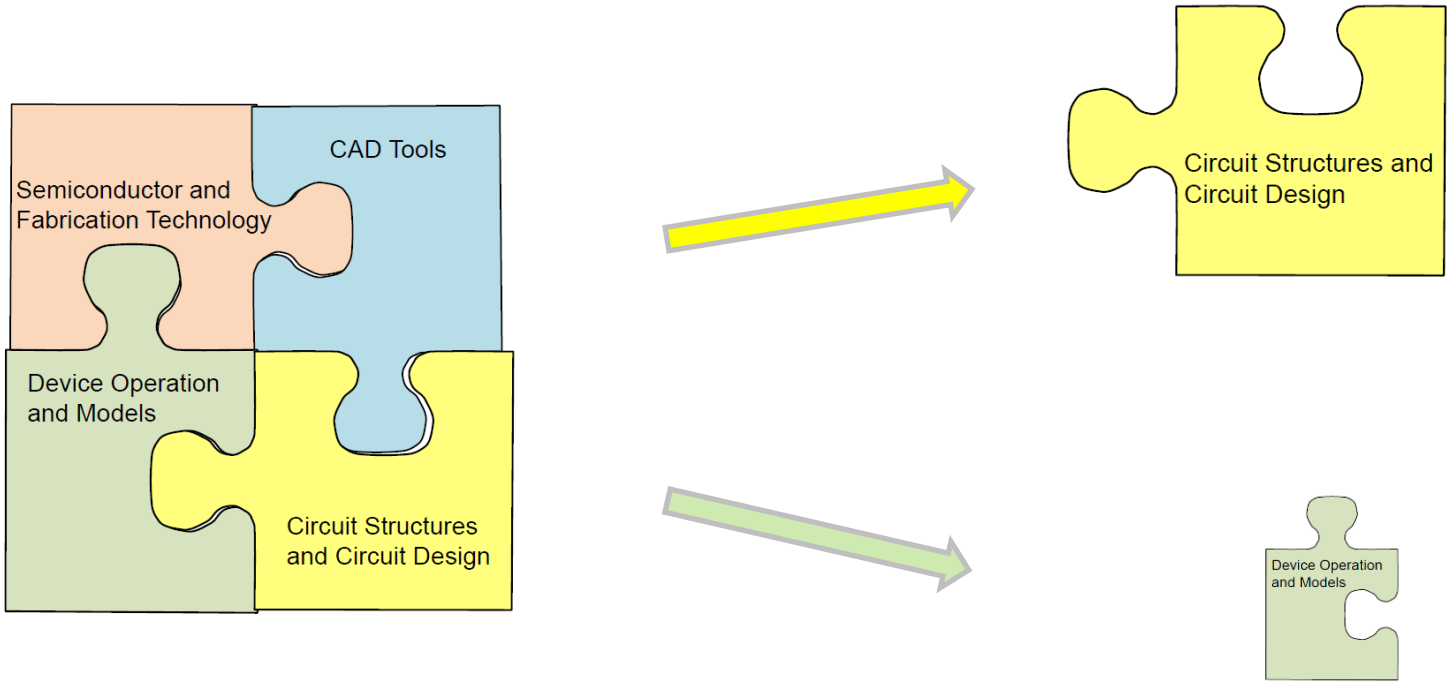
The Intel®4004 is a complete 4-bit parallel central processing unit (CPU). It is designed to be used in test systems, terminals, billing machines, process control and random logic replacement applications. The 4004 easily interfaces with keyboards, switches, displays, A-D converters, printers and other peripheral equipment.

The CPU can directly address 4K 8-bit instruction words of program memory and 5120 bits of data storage RAM. Sixteen index registers are provided for temporary data storage. Up to 16 4-bit input ports and 16 4-bit output ports may also be directly addressed.

The 4004 is fabricated with P-channel silicon gate MOS technology.



Basic Logic Circuits



Basic Logic Circuits

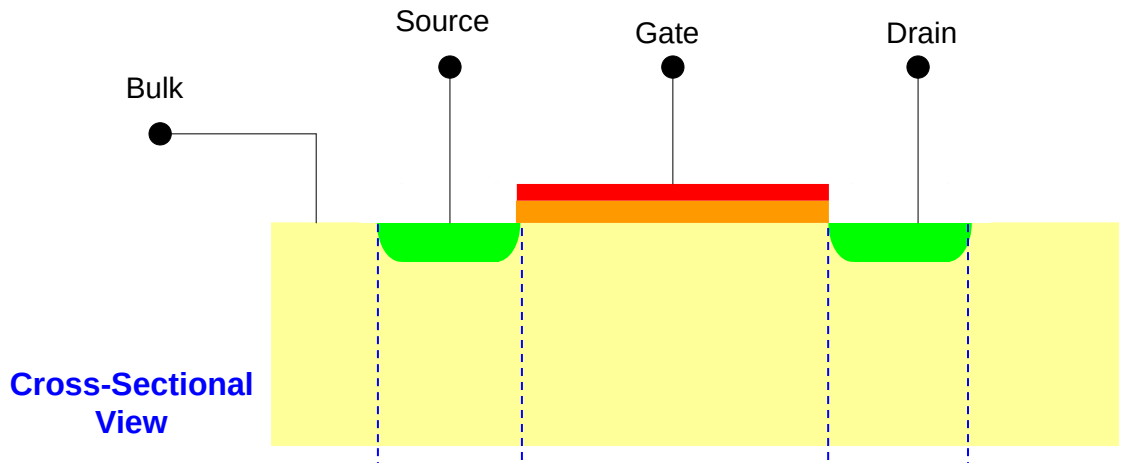
- Will present a brief description of logic circuits based upon simple models and qualitative description of processes
- Will later discuss process technology needed to develop better models
- Will even later provide more in-depth discussion of logic circuits based upon better device models

Models of Devices

- Several models of the electronic devices will be introduced throughout the course
  - Complexity
  - Accuracy
  - Insight
  - Application
- Will use the simplest model that can provide acceptable results for any given application

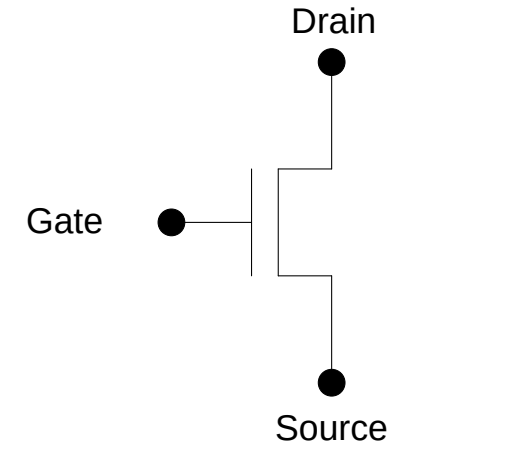
MOS Transistor

Qualitative Discussion of n-channel Operation



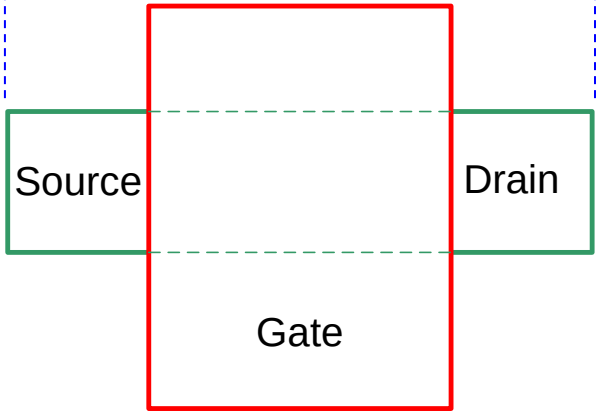
Cross-Sectional View

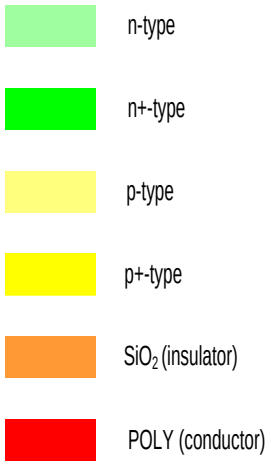
n-channel MOSFET



Symbol for n-channel MOSFET

Top View



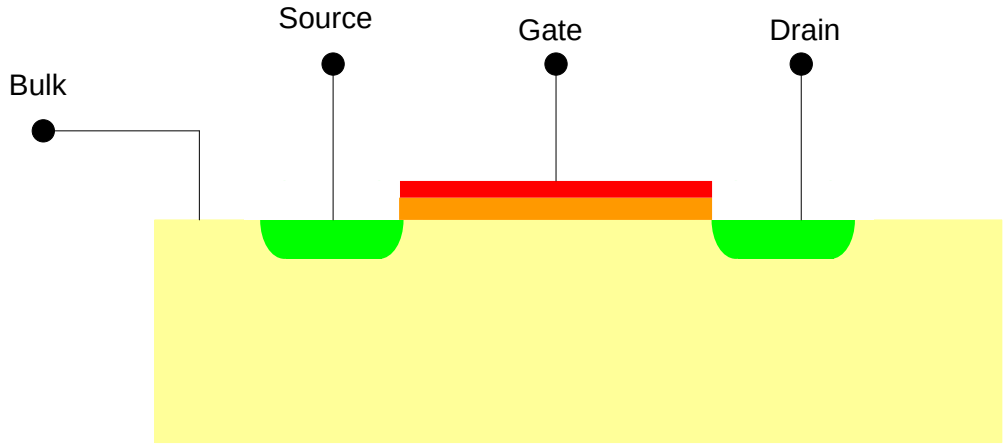


Designer always works with top view

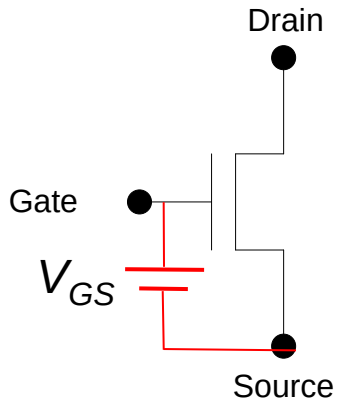
Complete Symmetry in construction between Drain and Source

MOS Transistor

Qualitative Discussion of n-channel Operation



n-channel MOSFET

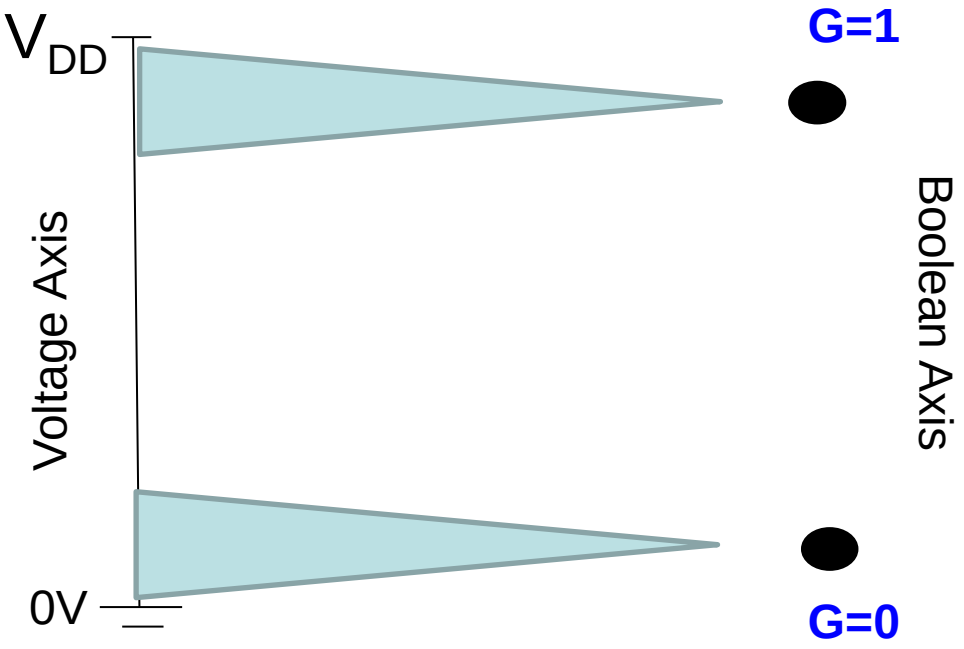


Behavioral Description of Operation of n-channel MOS Transistors Created for use in Basic Digital Circuits

If V_{GS} is large, short circuit exists between drain and source

If V_{GS} is small (or negative), open circuit exists between drain and source

Boolean/Continuous Notation:

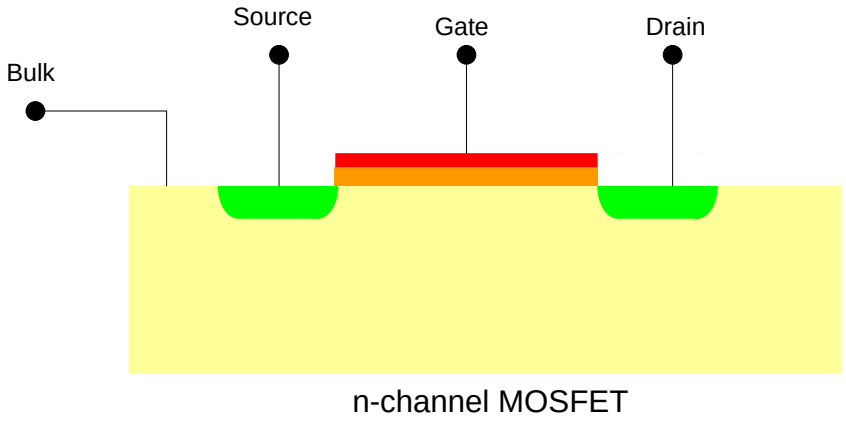


- **Voltage Axis is Continuous between 0V and V_{DD}**
- **Boolean axis is discrete with only two points**

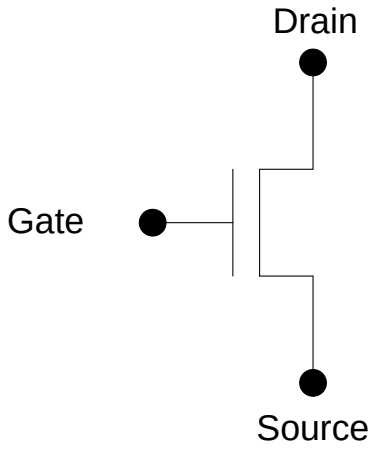
Most logic circuits characterized by the relationship between the Boolean input/output variables though these correspond to voltage intervals on the continuous voltage axis

MOS Transistor

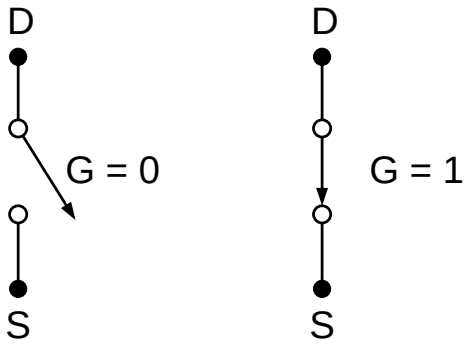
Qualitative Discussion of n-channel Operation



n-channel MOSFET



Equivalent Circuit for n-channel MOSFET

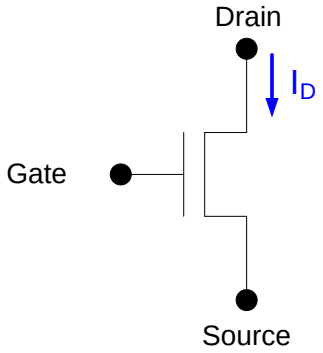


- Source assumed connected to (or close to) ground
- V_{GS}=0 denoted as Boolean gate voltage G=0
- V_{GS}=V_{DD} denoted as Boolean gate voltage G=1
- Boolean G is relative to ground potential

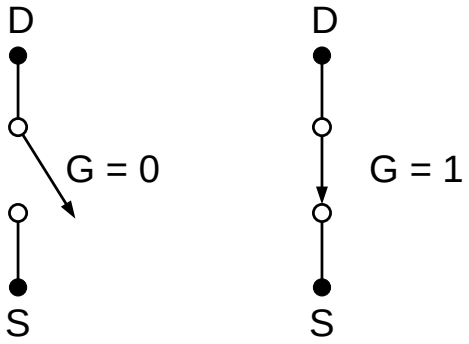
This is the first model we have for the n-channel MOSFET !

Ideal switch-level model

MOS Transistor MODEL



Equivalent Circuit for n-channel MOSFET with source as ground

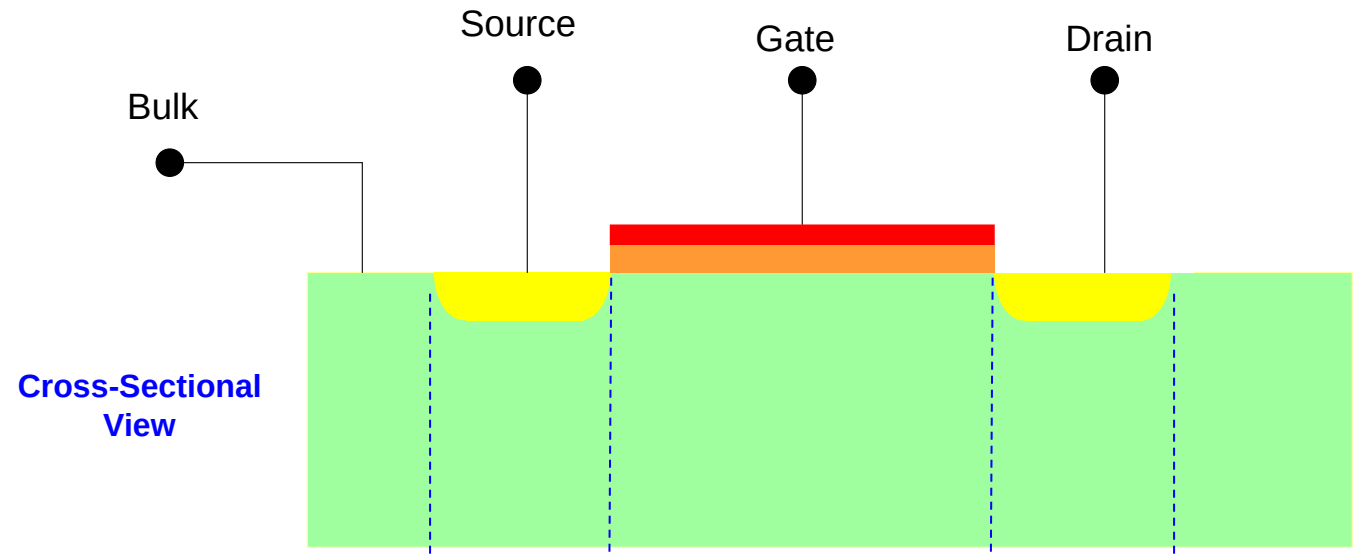


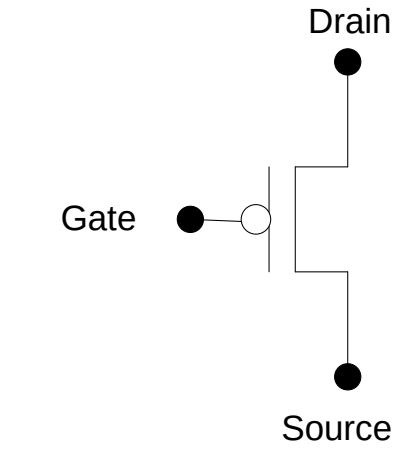
Mathematical model (not dependent upon Boolean notation):

$I_D = 0$	if V_{GS} is low (or negative)
$V_{DS} = 0$	if V_{GS} is high

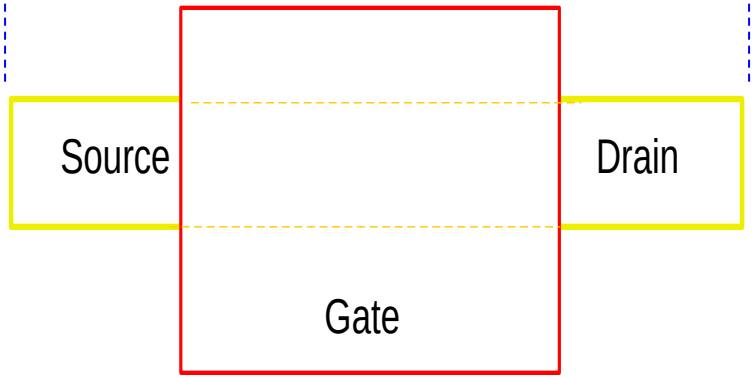
MOS Transistor

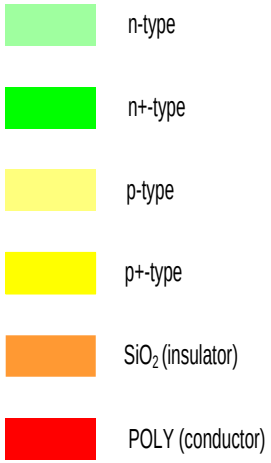
Qualitative Discussion of p-channel Operation





Symbol for p-channel MOSFET

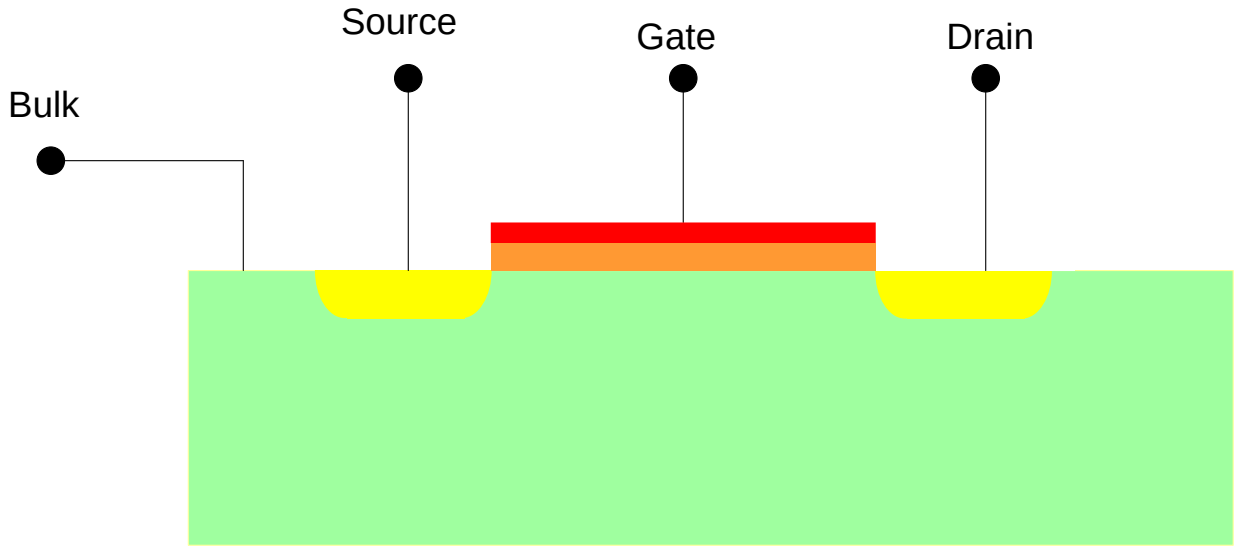


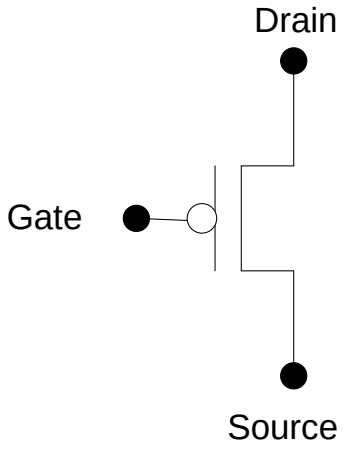


Complete Symmetry in construction between Drain and Source

MOS Transistor

Qualitative Discussion of p-channel Operation





p-channel MOSFET

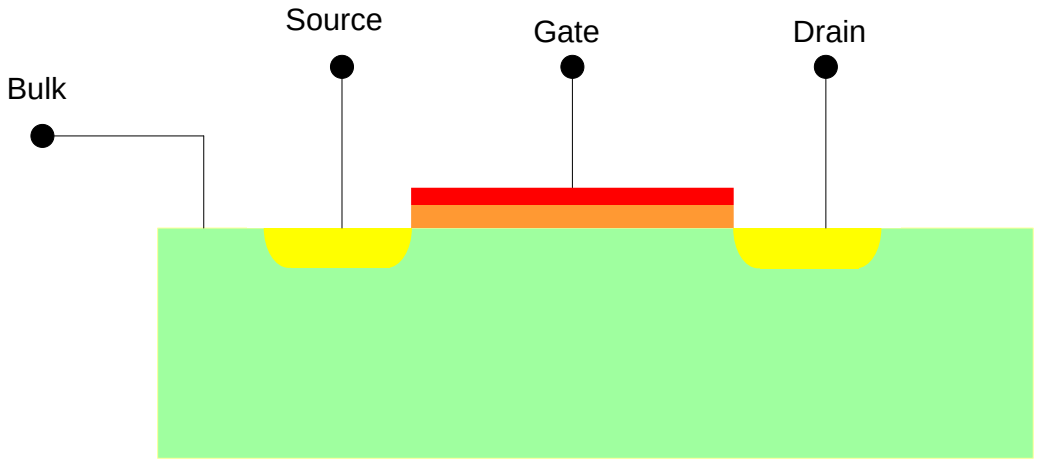
Behavioral Description of Operation of p-channel transistors created for use in basic digital circuits

If V_{GS} is large (and negative), short circuit exists between drain and source

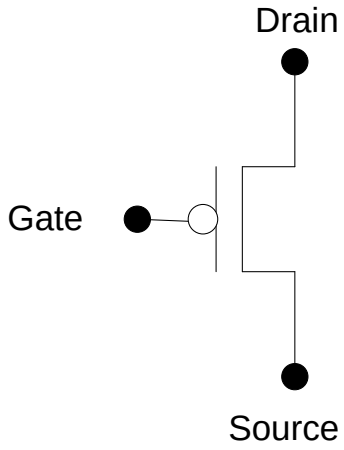
If V_{GS} is small (near 0 or positive), open circuit exists between drain and source

MOS Transistor

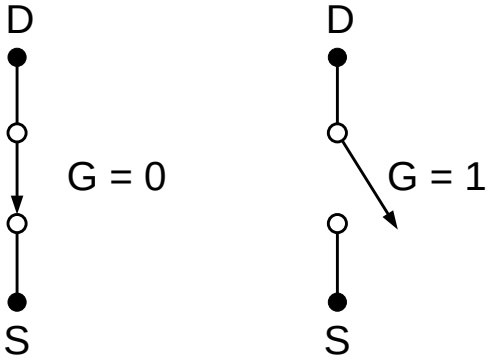
Qualitative Discussion of p-channel Operation



p-channel MOSFET



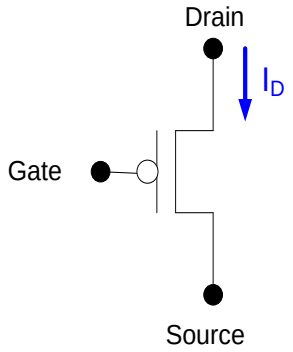
Equivalent Circuit for p-channel MOSFET



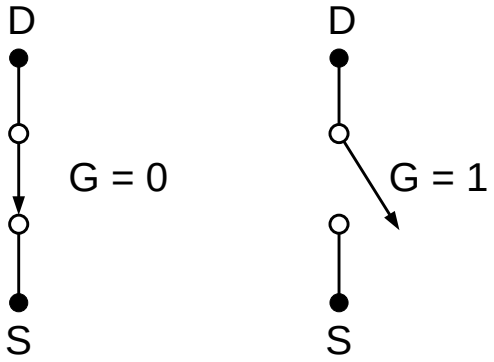
- Source assumed connected to (or close to) positive V_{DD}
- V_{GS}=0 denoted as Boolean gate voltage G=1
- V_{GS}= -V_{DD} denoted as Boolean gate voltage G=0
- Boolean G is relative to ground potential

This is the first model we have for the p-channel MOSFET !

MOS Transistor MODEL



Equivalent Circuit for p-channel MOSFET with Source at VDD



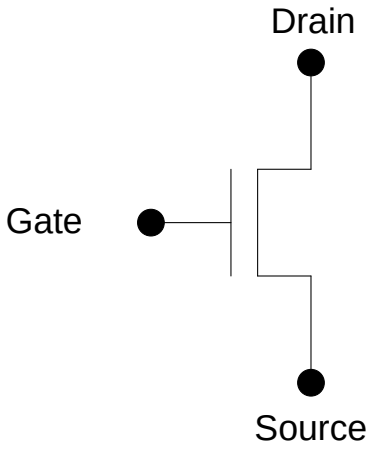
Mathematical model (not dependent upon Boolean notation):

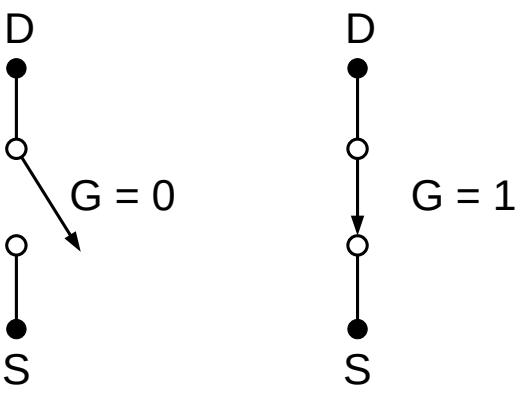
$I_D = 0$ if $|V_{GSp}|$ is small or V_{GSp} is positive

$V_{DS} = 0$ if $|V_{GSp}|$ is large

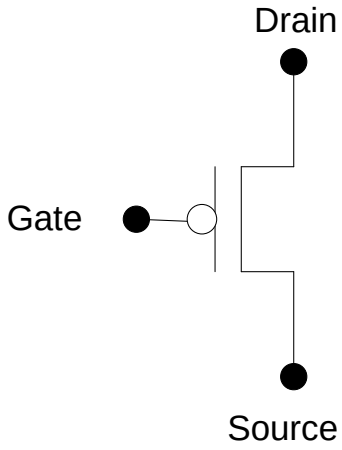
MOS Transistor

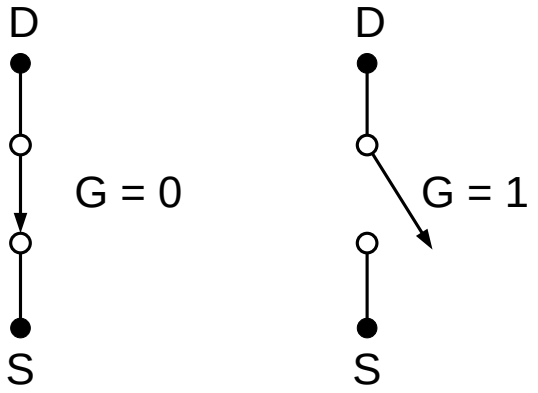
Comparison of Operation





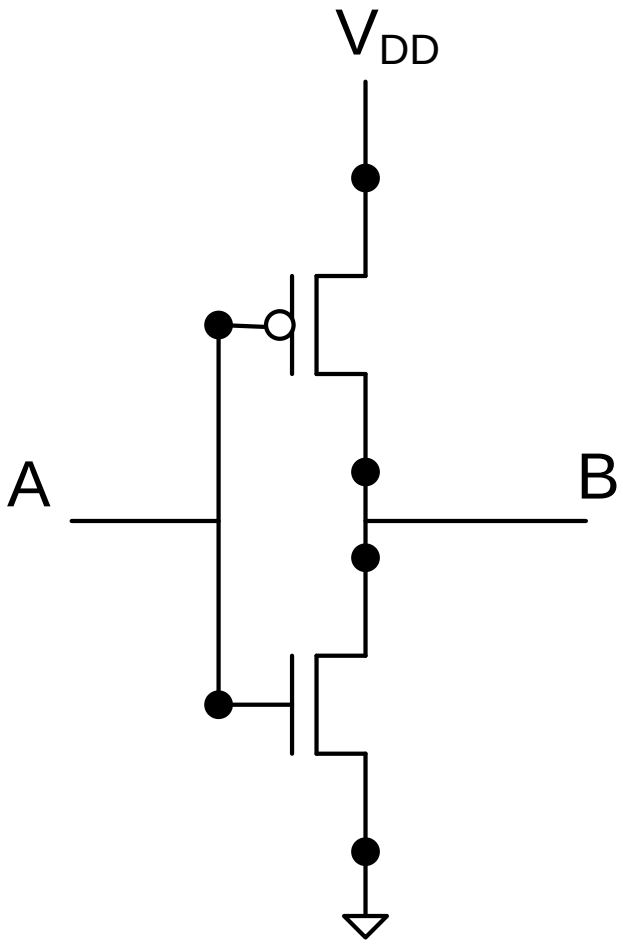
Source assumed connected to (or close to) ground

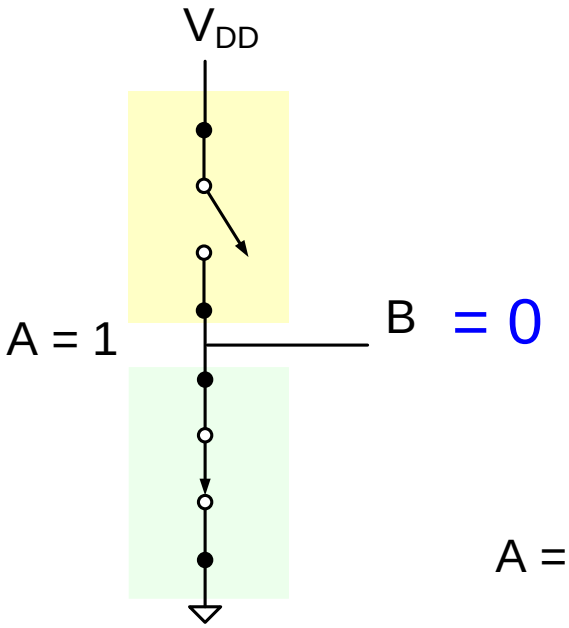


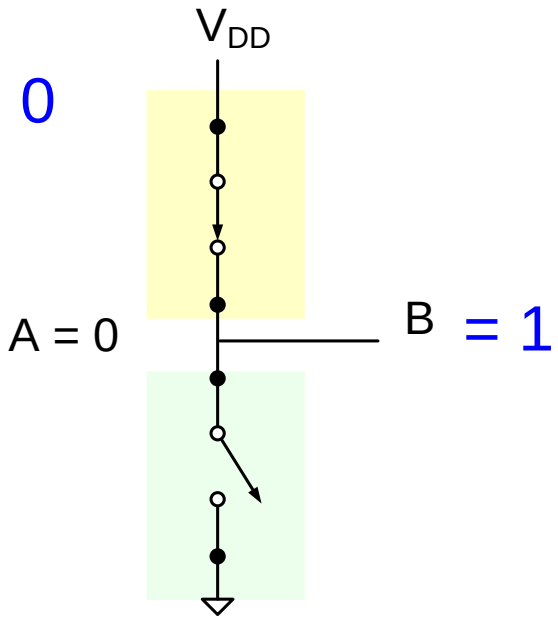


Source assumed connected to (or close to) positive V_{DD} and Boolean G at gate is relative to ground

Logic Circuits

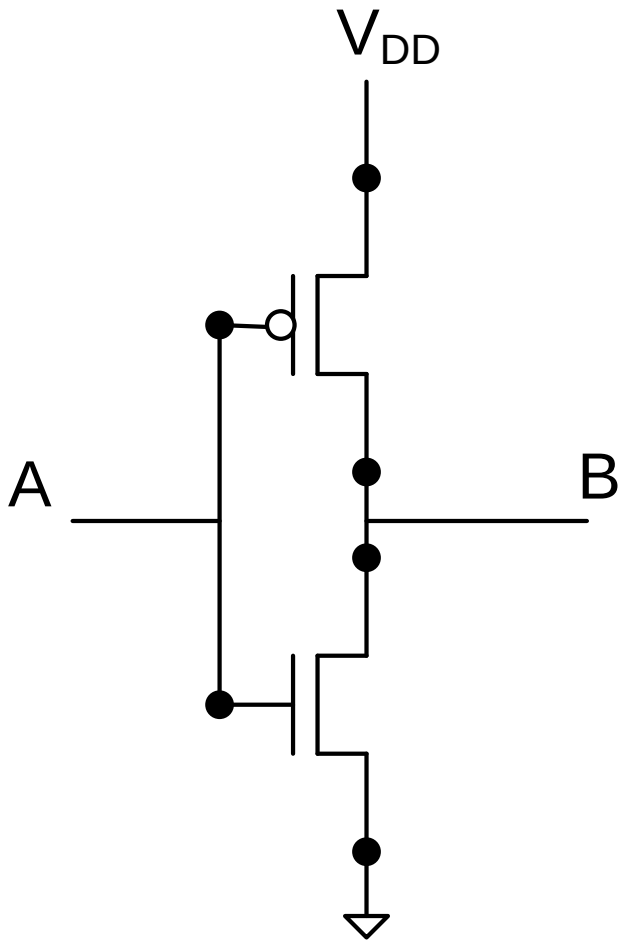






Circuit Behaves as a Boolean Inverter

Logic Circuits

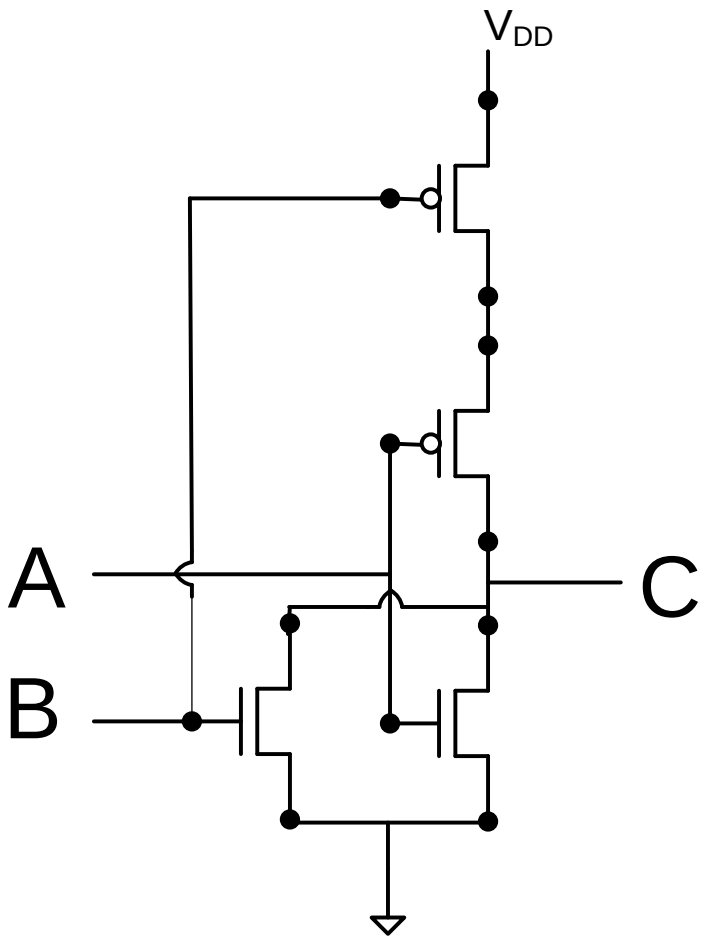


Inverter

Truth Table

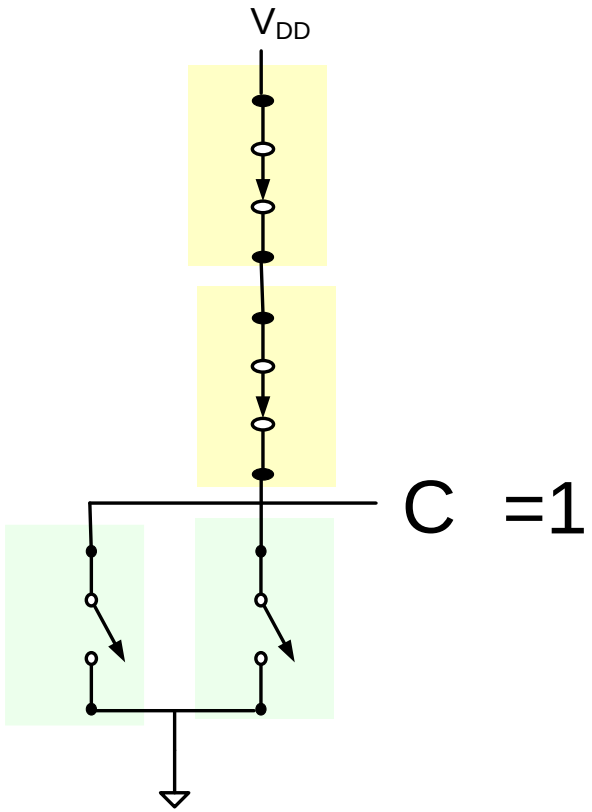
A	B
0	1
1	0

Logic Circuits

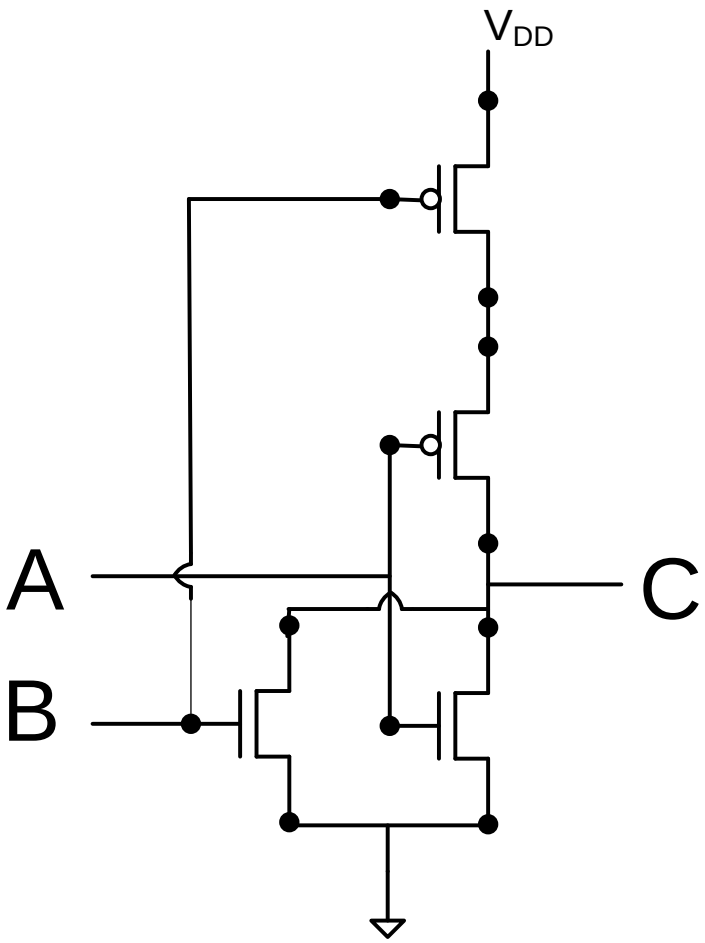


A=0

B=0

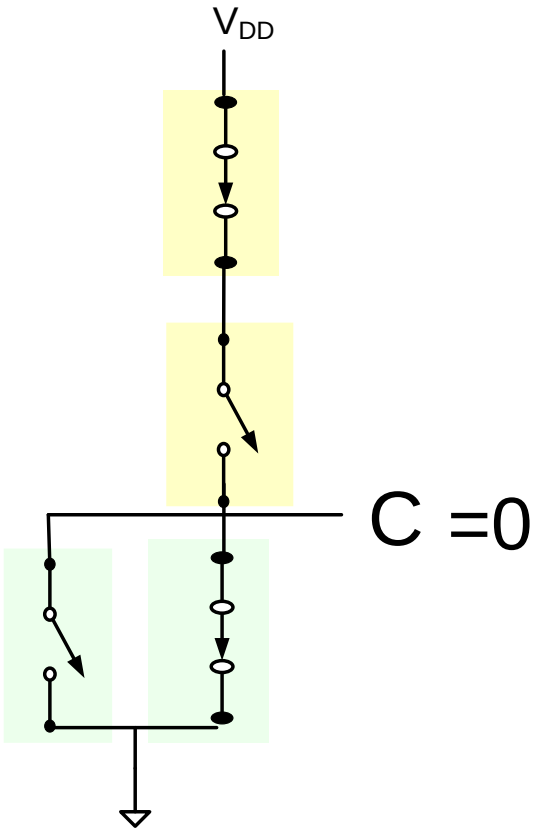


Logic Circuits

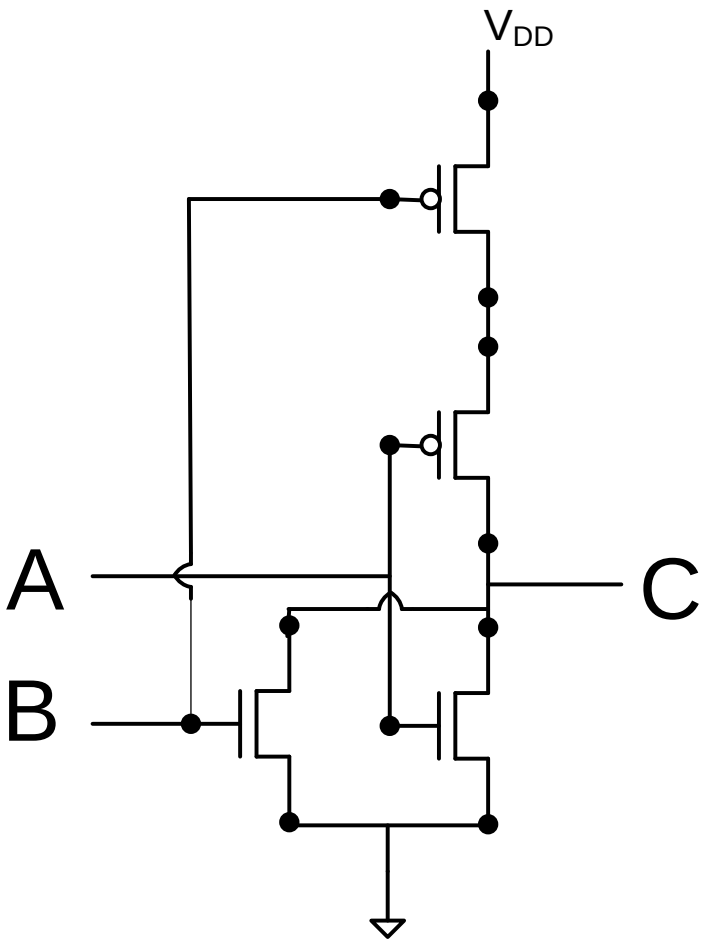


A=1

B=0

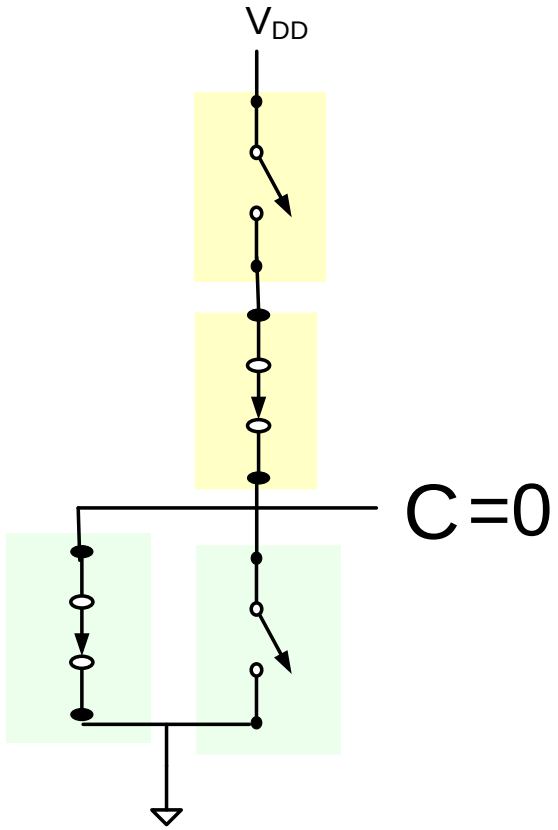


Logic Circuits

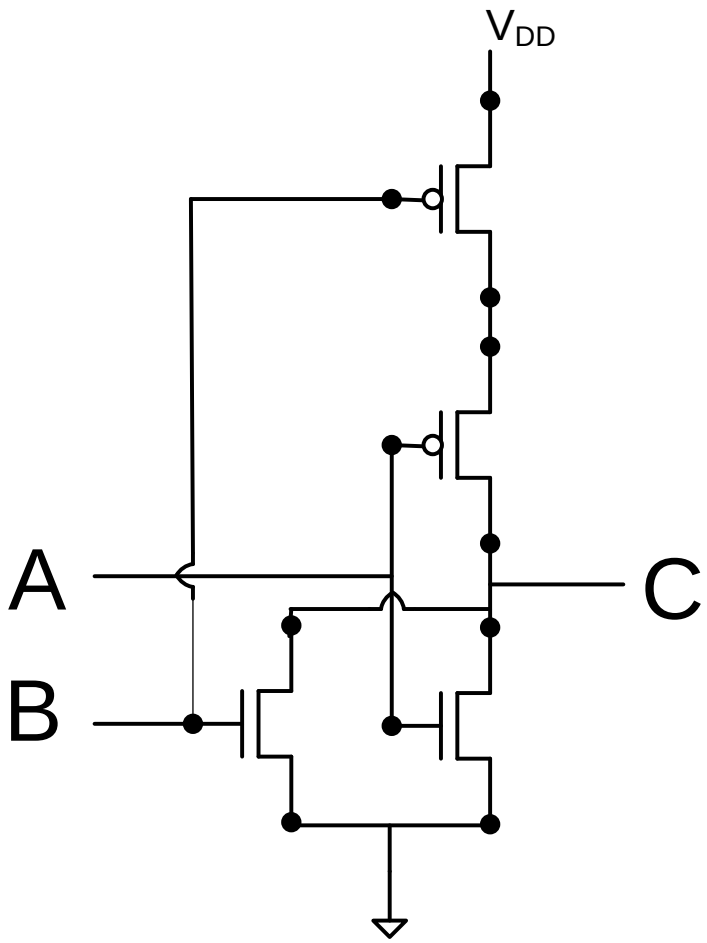


A=0

B=1

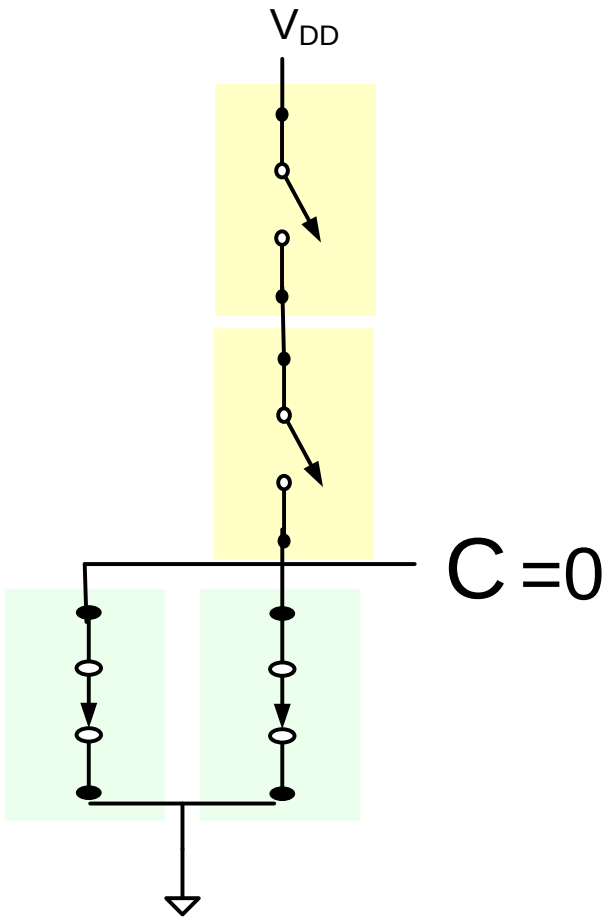


Logic Circuits

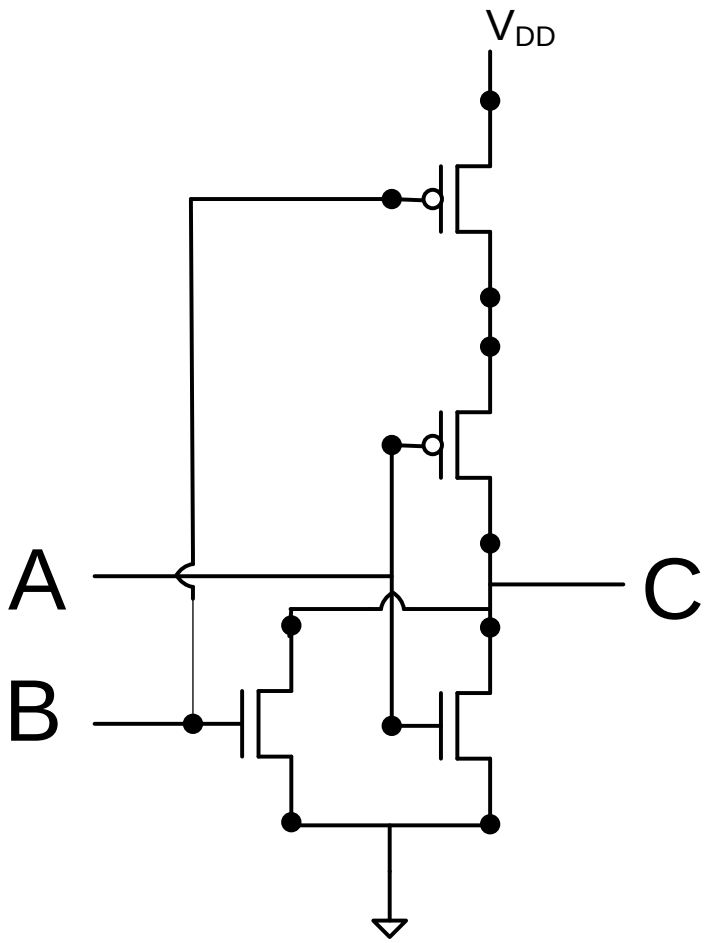


A=1

B=1



Logic Circuits

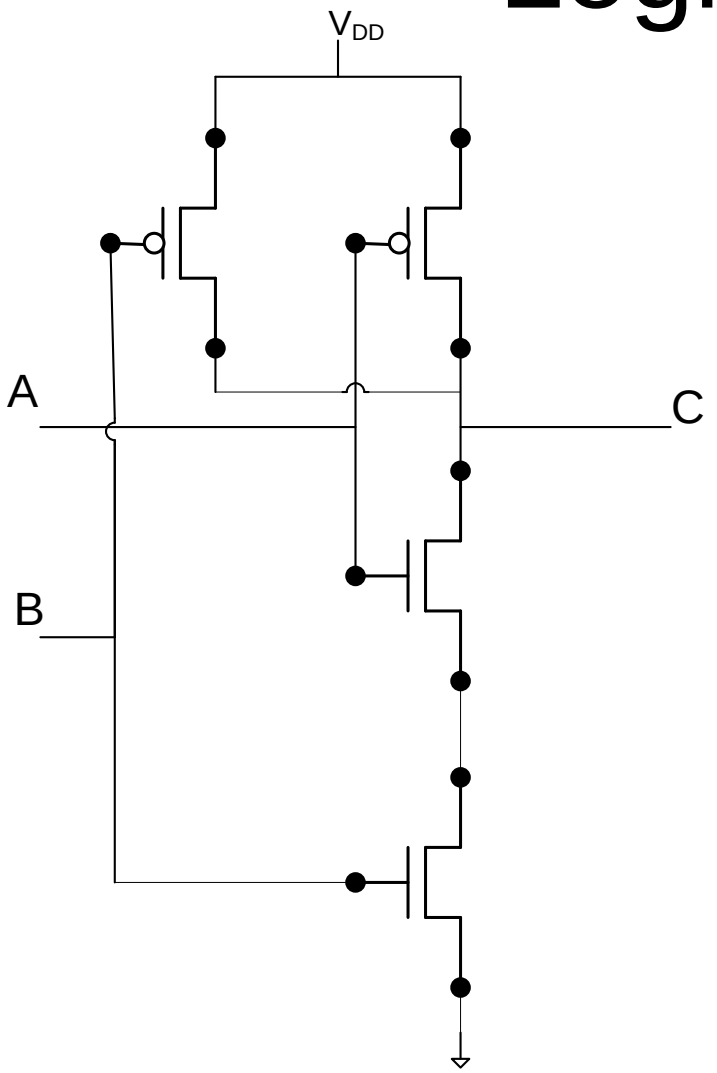


NOR Gate

Truth Table

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

Logic Circuits

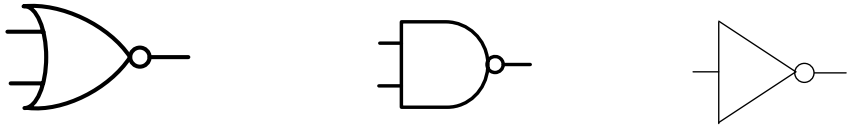


NAND Gate

Truth Table

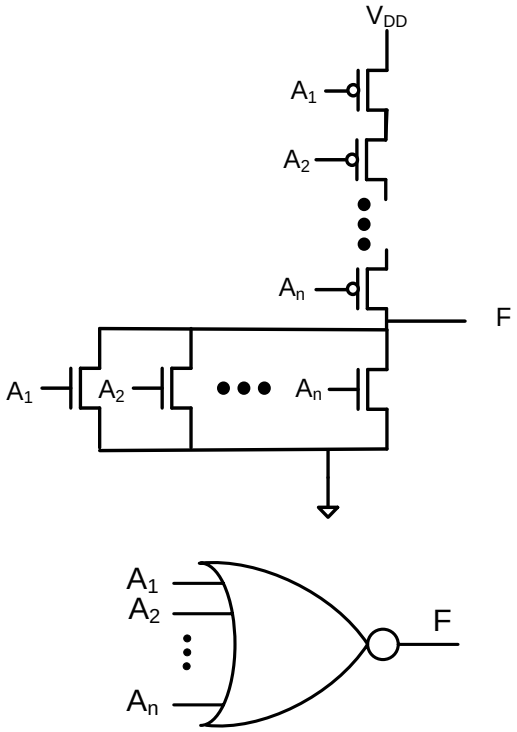
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

Logic Circuits

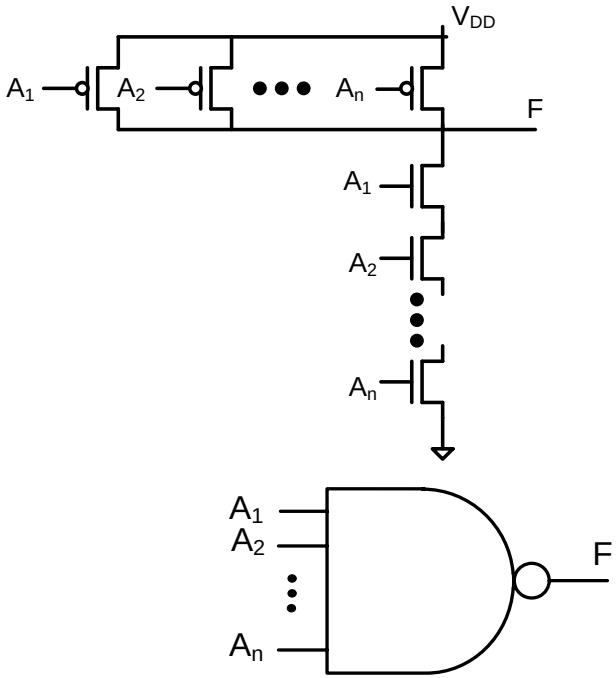


Approach can be extended to arbitrary number of inputs

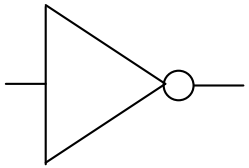
n-input NOR gate

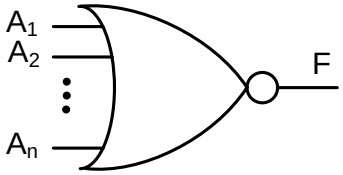


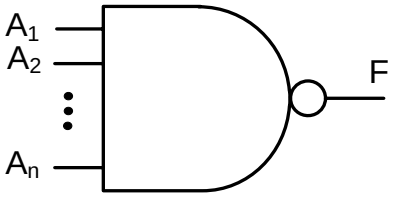
n-input NAND gate



Complete Logic Family







Family of n-input NOR gates forms a complete logic family

Family of n-input NAND gates forms a complete logic family

Having both NAND and NOR gates available is a luxury

Can now implement any combinational logic function !!

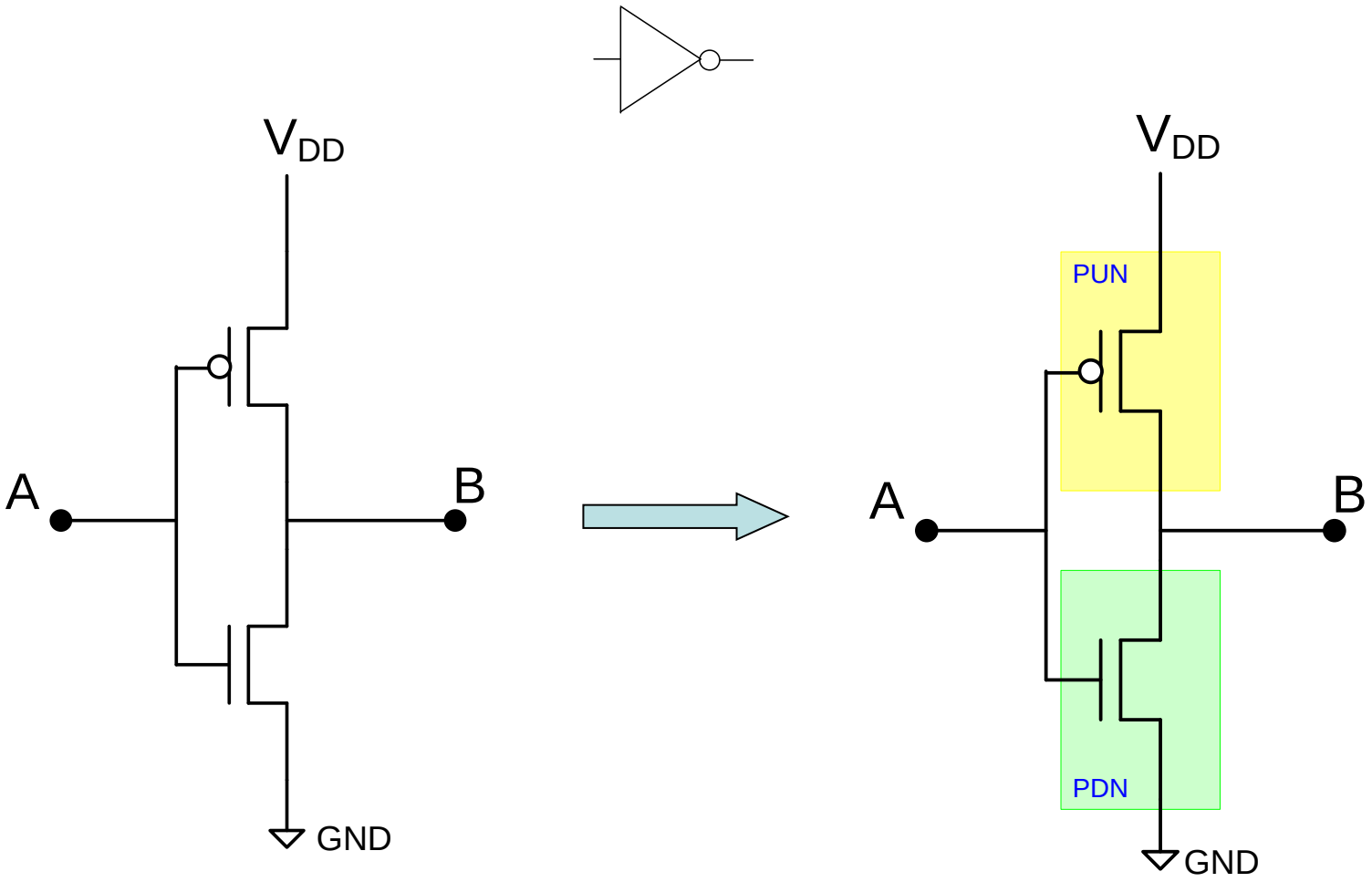
If add one flip flop, can implement any Boolean system !!

Flip flops easy to design but will discuss sequential logic systems later

Other logic circuits

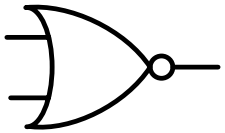
- Other methods for designing logic circuits exist
- Insight will be provided on how other logic circuits evolve
- Several different types of logic circuits are often used simultaneously in any circuit design

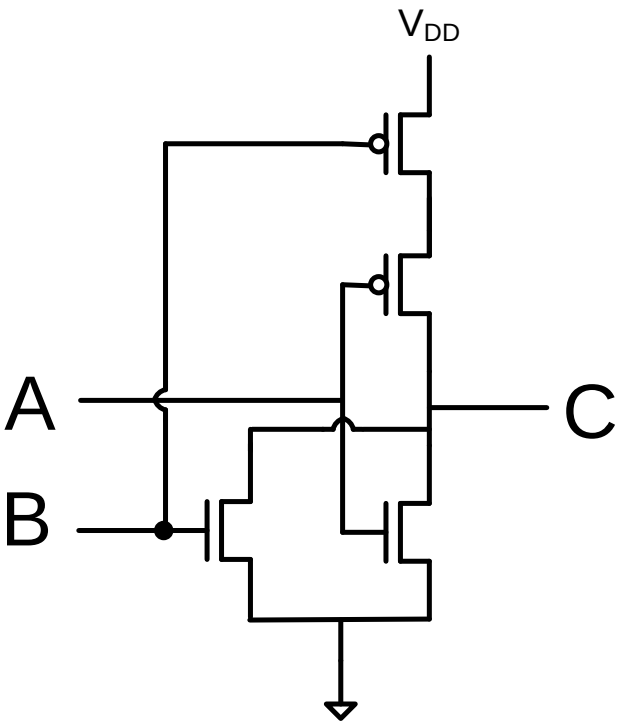
Pull-up and Pull-down Networks

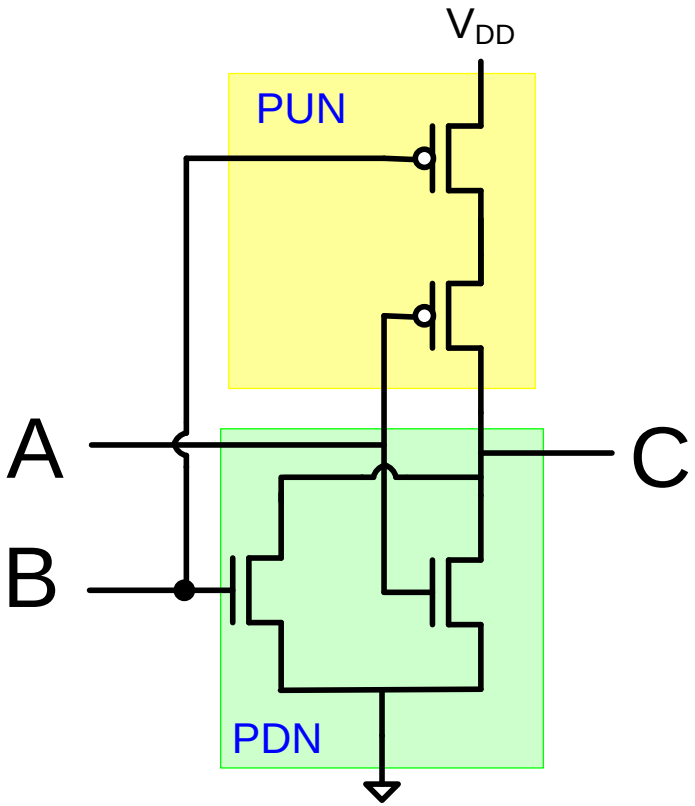


PU network comprised of p-channel device and “tries” to pull B to VDD when conducting
PD network comprised of n-channel device and “tries to pull B to GND when conducting
One and only one of these networks is conducting at the same time (to avoid contention)

Pull-up and Pull-down Networks

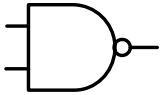


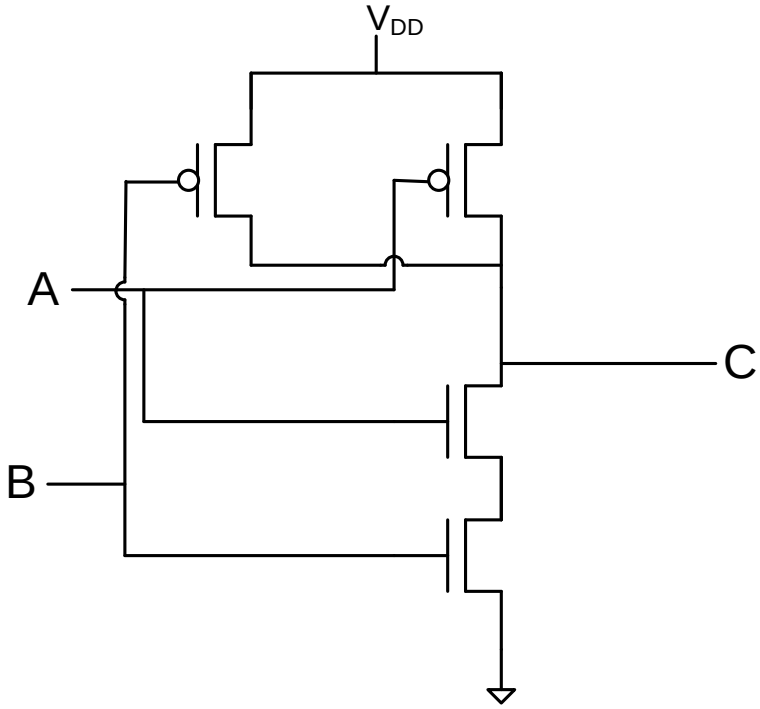


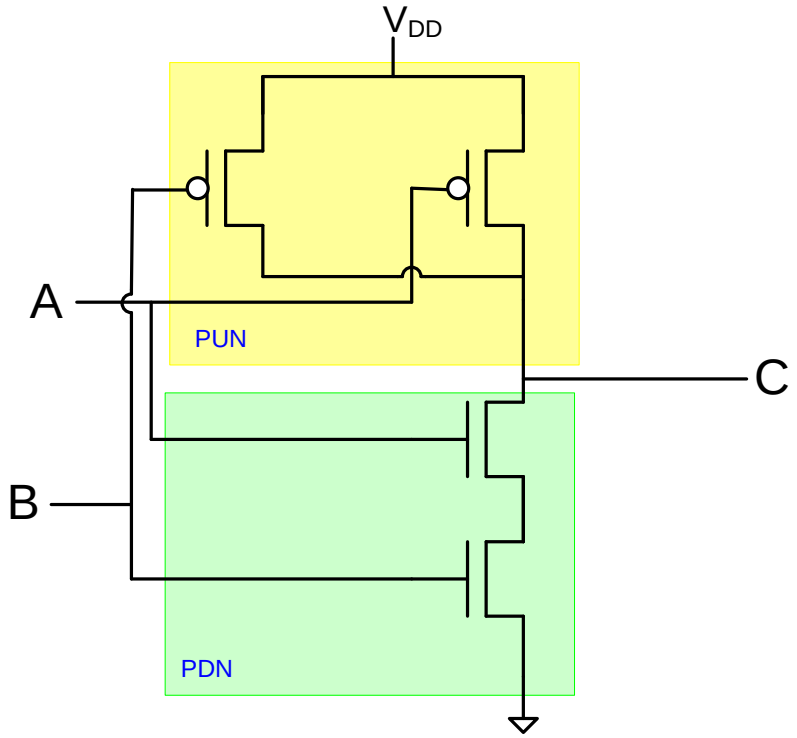


PU network comprised of p-channel devices
PD network comprised of n-channel devices
One and only one of these networks is conducting at the same time

Pull-up and Pull-down Networks

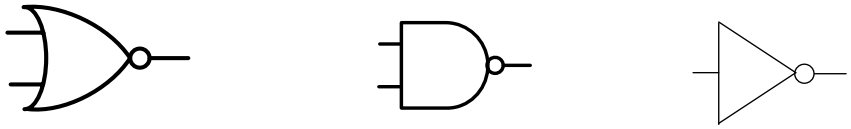






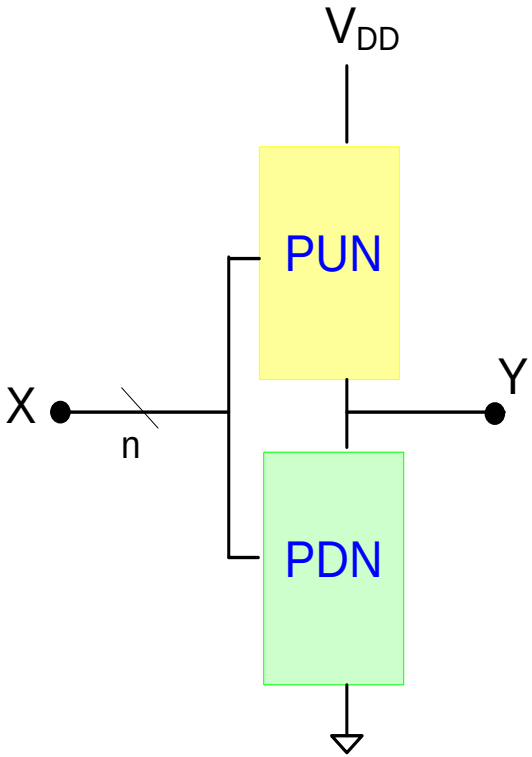
PU network comprised of p-channel devices
PD network comprised of n-channel devices
One and only one of these networks is conducting at the same time

Pull-up and Pull-down Networks



In these circuits, the PUN and PDN have the 3 interesting characteristics

1. PU network comprised of p-channel devices
2. PD network comprised of n-channel devices
3. One and only one of these networks is conducting at the same time



What are V_H and V_L?
What is the power dissipation?
How fast are these logic circuits?

Stay Safe and Stay Healthy !

End of Lecture 5